# Table of Contents

1. Introduction to Digital Logic
   1.1 Background  
   1.2 Digital Logic  
   1.3 Verilog  

2. Basic Logic Gates  
   2.1 Truth Tables and Logic Equations  
      The Three Basic Gates  
      Four New Gates  
   2.2 Positive and Negative Logic: De Morgan’s Theorem  
   2.3 Sum of Products Design  
   2.4 Product of Sums Design  
      Verilog Examples  
      Example 1 – 2-Input Gates  
      Example 2 – Multiple-Input Gates  
      Problems  

3. Boolean Algebra and Logic Equations  
   3.1 Boolean Theorems  
      One-Variable Theorems  
      Two- and Three-Variable Theorems  
   3.2 Karnaugh Maps  
      Two-Variable K-Maps  
      Three-Variable K-Maps  
      Four-Variable K-Maps  
   3.3 Computer Minimization Techniques  
      Tabular Representations  
      Prime Implicants  
      Essential Prime Implicants  
      Verilog Examples  
      Example 3 – Majority Circuit  
      Example 4 – 2-Bit Comparator  
      Problems  

4. Implementing Digital Circuits  
   4.1 Implementing Gates  
   4.2 Transistor-Transistor Logic (TTL)  
   4.3 Programmable Logic Devices (PLDs and CPLDs)  
      A 2-Input, 1-Output PLD
5. **Combinational Logic**

5.1 **Multiplexers**
- 2-to-1 Multiplexer
- 4-to-1 Multiplexer
- Quad 2-to-1 Multiplexer

Verilog Examples
- Example 6 – 2-to-1 Multiplexer: *if* Statement
- Example 7 – 4-to-1 Multiplexer: Module Instantiation
- Example 8 – 4-to-1 Multiplexer: *case* Statement
- Example 9 – A Quad 2-to-1 Multiplexer
- Example 10 – Generic Multiplexer: Parameters
- Example 11 – Glitches

5.2 **7-Segment Displays**

Verilog Examples
- Example 12 – 7-Segment Decoder: Logic Equations
- Example 13 – 7-Segment Decoder: *case* Statement
- Example 14 – Multiplexing 7-Segment Displays
- Example 15 – 7-Segment Displays: *x7seg* and *x7segb*

5.3 **Comparators**
- Cascading Comparators
- TTL Comparators

Verilog Examples
- Example 16 – 4-Bit Comparator Using a Verilog Task
- Example 17 – *N*-Bit Comparator Using Relational Operators

5.4 **Decoders and Encoders**
- Decoders
- TTL Decoders
- Encoders
- Priority Encoders
- TTL Encoders

Verilog Examples
- Example 18 – 3-to-8 Decoder: Logic Equations
- Example 19 – 3-to-8 Decoder: *for* Loops
- Example 20 – 8-to-3 Encoder: Logic Equations
- Example 21 – 8-to-3 Encoder: *for* Loops
- Example 22 – 8-to-3 Priority Encoder

5.5 **Code Converters**
- Binary-to-BCD Converters
- Shift and Add 3 Algorithm
6. Arithmetic Circuits

6.1 Adders
   - Half Adder
   - Full Adder
   - Carry and Overflow
   - TTL Adder
   Verilog Examples
   - Example 27 – 4-Bit Adder: Logic Equations
   - Example 28 – 4-Bit Adder: Behavioral Statements
   - Example 29 – N-Bit Adder: Behavioral Statements

6.2 Subtractors
   - Half Subtractor
   - Full Subtractor
   - An Adder/Subtractor Circuit
   Verilog Examples
   - Example 30 – 4-Bit Adder/Subtractor: Logic Equations
   - Example 31 – N-Bit Subtractor: Behavioral Statements

6.3 Shifters
   Verilog Examples
   - Example 32 – 4-Bit Shifter

6.4 Multiplication
   - Binary Multiplication
   - Signed Multiplication
   Verilog Examples
   - Example 33 – Multiplying by a Constant
   - Example 34 – A 4-Bit Multiplier

6.5 Division
   - Binary Division
   Verilog Examples
   - Example 35 – An 8-Bit Divider using a Task

6.6 Arithmetic Logic Unit (ALU)
   Verilog Examples
   - Example 36 – 4-Bit ALU

Problems

7. Sequential Logic

7.1 Latches and Flip-Flops
   - SR Latch
Clocked SR Latch 153
D Latch 153
Edge-Triggered D Flip-Flop 154

Verilog Examples 156
Example 37 – Edge-Triggered D Flip-Flop 156
Example 38 – Edge-Triggered D Flip-Flop with Set and Clear 157
Example 39 – D Flip-Flops in Verilog 158
Example 40 – D Flip-Flop with Asynchronous Set and Clear 159
Example 41 – Divide-by-2 Counter 160

7.2 Registers 161
Verilog Examples 163
Example 42 – 1-Bit Register 163
Example 43 – 4-Bit Register 164
Example 44 – N-Bit Register 165

7.3 Shift Registers 166
4-Bit Ring Counter 167
Verilog Examples 167
Example 45 – Shift Registers 167
Example 46 – Ring Counter 168
Example 47 – Debounce Pushbuttons 169
Example 48 – Clock Pulse 171

7.4 Counters 173
Arbitrary Waveform 174
Verilog Examples 175
Example 49 – 3-Bit Counter 175
Example 50 – Modulo-5 Counter 177
Example 51 – N-Bit Counter 178
Example 52 – Clock Divider: Modulo-10K Counter 180
Example 53 – Arbitrary Waveform 184

7.5 Pulse-Width Modulation (PWM) 185
Controlling the Speed of a DC Motor using PWM 186
Controlling the Position of a Servo using PWM 187
Verilog Examples 188
Example 54 – Pulse-Width Modulation (PWM) 188
Example 55 – PWM Signal for Controlling Servos 190

7.6 BASYS/Nexys-2 Board Examples 191
Verilog Examples 191
Example 56 – Loading Switch Data into a Register 191
Example 57 – Shifting Data into a Shift Register 193
Example 58 – Scrolling the 7-Segment Display 195
Example 59 – Fibonacci Sequence 200

Problems 203

8. State Machines 206
8.1 Mealy and Moore State Machines 206
8.2 A Moore Machine Sequence Detector 207
8.3 Mealy Machine Sequence Detector 209
Verilog Examples 210
  Example 60 – Sequence Detector 210
  Example 61 – Door Lock Code 215
  Example 62 – Traffic Lights 219
Problems 224

9. Datapaths and Control Units 225
  9.1 Verilog while Statement 225
    Example 63 – GCD Algorithm – Part 1 225
  9.2 Datapaths and Control Units 227
    Example 64 – GCD Algorithm – Part 2 229
    Example 65 – An Integer Square Root Algorithm 237

10. Integrating the Datapath and Control Unit 247
    Example 66 – GCD Algorithm – Part 3 249
    Example 67 – Integer Square Root – Part 2 253

11. Memory 257
    Example 68 – A Verilog ROM 257
    Example 69 – Distributed RAM/ROM 262
    Example 70 – Block RAM/ROM 267

12. VGA Controller 271
    Example 71 – VGA-Stripes 275
    Example 72 – VGA-PROM 281
    Example 73 – Sprites in Block ROM 286
    Example 74 – Screen Saver 292

13. PS/2 Port 297
    Example 75 – Keyboard 300
    Example 76 – Mouse 307

Appendix A – Aldec Active-HDL Tutorial 316
  Part 1: Project Setup 316
  Part 2: Design Entry 320
  Part 3: Simulation 323
  Part 4: Creating a Top-level Design 327
  Part 5: Synthesis and Implementation 329
  Part 6: Program FPGA Board 333

Appendix B – Number Systems 334
  B.1 Counting in Binary and Hexadecimal 334
  B.2 Positional Notation 338
  B.3 Fractional Numbers 339
  B.4 Number System Conversions 339
B.5 Negative Numbers  343

Appendix C – Making a Turnkey System  347

Appendix D – Digilent FPGA Boards Comparison Chart  349

Appendix E – Installing the Xilinx ISE/WebPACK, Aldec Active-HDL, and Digilent Adept2 Software  350

Appendix F – Verilog Quick Reference Guide  352