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(This page outlines the Xilinx ® proprietary USB 2.0 layout/interface.)
VCC for Bank 0 is set by JP9 on Sheet 9

VCC for Bank 1 = 3.3V

Notes are for pins that vary between 500/1200/1600 dies

Spartan 3E Starter Board
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Sheet: XC3SE Banks 0 and 1, Clock ICs
Author: GMA

Title: 3E Starter
Rev: D
Doc#: 500-087
Date: 02/08/06
Sheet: 7/14
NOTE: Termination network for IC20, the MT46U16M16TG-75 on sheet 14