Unused banks on the LX50T and SX50T
System Clock Generation

User Clock

Diff Clocks: SMAs, Generation, MUX and Buffer
The PHY MDIP Pins below are Media Dependent Interface Pins (MDIP), and are all bidirectional pins.

**Title:** 10/100/1000 PHY  
**Sheet:** 14 of 27  
**Drawn By:**
VGA Out Codec

IIC Address = 0x76
The burst order mode of the SRAM is set to "Linear" by default.
5v to 3.3V Regulator

5v to 1.0V Regulator

5v to 1.8V Regulator

5V Power Synchronizing Circuit

5V Power - Jack, Switch and LED

5V Power Supplies