Atlys AXI HDMI IP Core v1.00

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Introduction

This document describes the Atlys AXI (Advanced eXtensible Interface) HDMI (High-Definition Multimedia Interface) Intellectual Property. This IP provides high-bandwidth direct memory access between HDMI port and memory, thru AXI4-Stream, using Xilinx VDMA Core.

Features

- AXI4-Stream compliant
- Dynamic resolution change, thru AXI4-Lite slave interface
- Independent, asynchronous channel operation
- 24bits/pixel
- Resolutions supported: 640x480/60Hz, 480p60, 800x600/60Hz, 720p60, 1600x900/60Hz

Functional Description

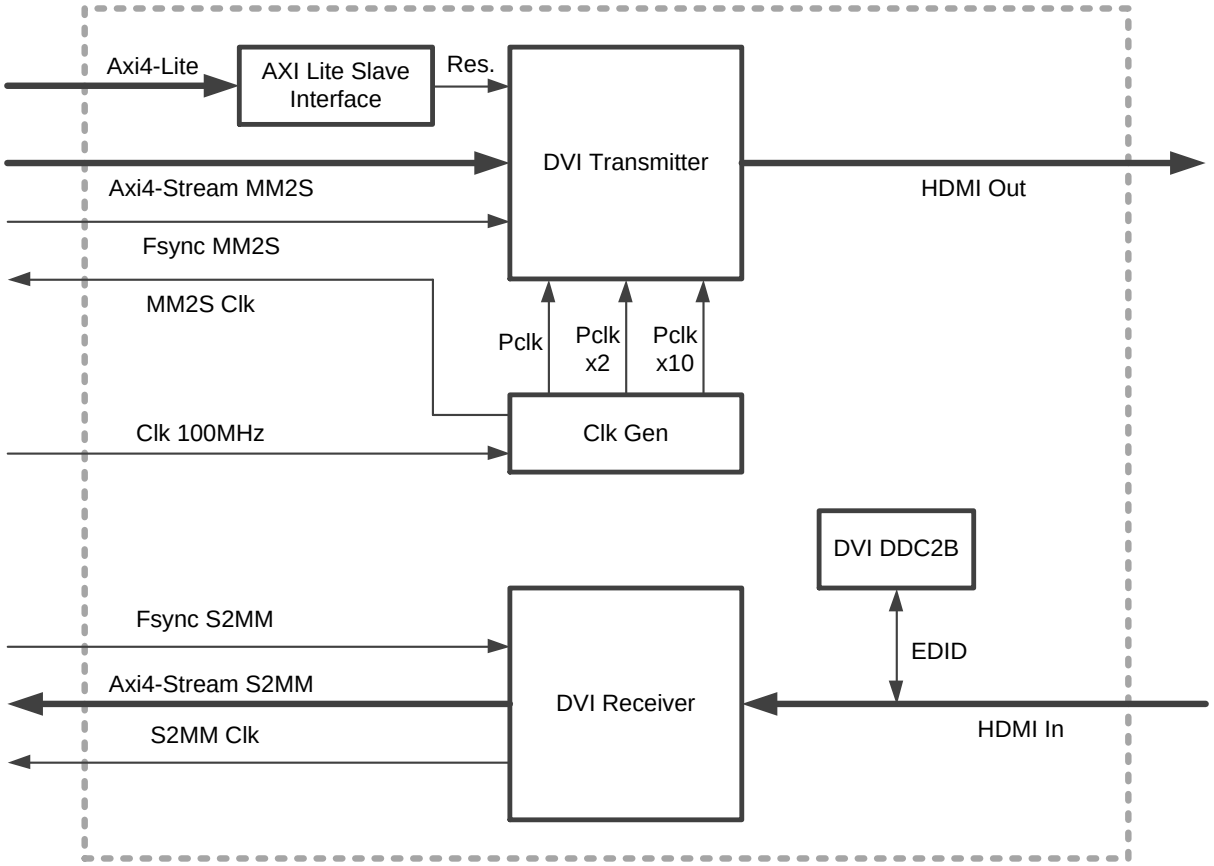


Figure 1. AXI HDMI Block Diagram

The Atlys AXI HDMI consists of a Clk Gen module, for generating pixel clock and the serialization clock, with a 100MHz input clock. It also generates MM2S clock for controlling the MM2S AXI4-Stream interface's clock (of AXI VDMA). An AXI Lite Slave Interface is used for setting the resolution to display on HDMI Out. DVI Receiver decodes the HDMI In when FSync S2MM pulse

is received from AXI VDMA. It also has a read-only DDC2B (Display Data Channel) for providing to the source the EDID (Extended Display Identification Data).

The DVI Receiver and DVI Transmitter interface Xilinx AXI VDMA thru two 32-bit wide AXI4-Stream interfaces.

I/O Signals

The AXI HDMI I/O signals are listed and described in Table 1.

Table 1. AXI HDMI I/O Signal Description

Signal Name	Interface	Signal Type	Init Status	Description
aclk	Clock	I	-	AXI HDMI general clock. Must be greater of equal to the mm2s_dcm_aclk_100mhz.
s_axi_aclk	AXI Lite	I	-	AXI Lite Slave Interface's clock.
mm2s_dcm_aclk_100mhz	Clk Gen	I	-	Clk Gen module clock for the internal DCM. Must be 100MHz.
s_axis_mm2s_aclk	MM2S	O	-	AXI DVI Transmitter module clock output.
s_axis_s2mm_aclk	S2MM	O	-	AXI DVI Receiver module clock output.
Global Signals				
mm2s_fsync_in	MM2S	I	-	MM2S Flame Sync Input. Asserts high for 1 s_axis_mm2s_aclk cycle with each flame boundary.
mm2s_buffer_almost_empty	MM2S	I	-	AXI VDMA MM2S Line Buffer Almost Empty. Indicates the MM2S line buffer has C_MM2S_LINEBUFFER_THRESH bytes of less stored.
s2mm_fsync_in	S2MM	I	-	S2MM Flame Sync Input. Asserts high for 1 s_axis_s2mm_aclk cycle with each flame boundary.
AXI4-Lite Interface Signals				
s_axi_aresetn	AXI Lite	I	-	AXI4-Lite Reset, active low.
s_axi_awaddr (C_S_AXI_ADDR_WIDTH-1:0)	AXI Lite	I	-	AXI4-Lite Write Address Bus.

Signal Name	Interface	Signal Type	Init Status	Description
s_axi_awvalid	AXI Lite	I	-	AXI4-Lite Write Address Channel Write Address Valid. • 1 = Write address is valid. • 0 = Write address is not valid.
s_axi_wdata (C_S_AXI_DATA_WIDTH-1:0)	AXI Lite	I	-	AXI4-Lite Write Data Bus.
s_axi_wstrb ((C_S_AXI_DATA_WIDTH/8)-1:0)	AXI Lite	I	-	AXI4-Lite Write Strobes. Indicates which byte lanes to update.
s_axi_wvalid	AXI Lite	I	-	AXI4-Lite Write Data Channel Write Data Valid. • 1 = Write data is valid. • 0 = Write data is not valid.
s_axi_bready	AXI Lite	I	-	AXI4-Lite Write Response Channel Ready. Indicates target is ready to receive response. • 1 = Ready to receive response. • 0 = Not ready to receive response.
s_axi_araddr (C_S_AXI_ADDR_WIDTH-1:0)	AXI Lite	I	-	AXI4-Lite Read Address Bus.
s_axi_arvalid	AXI Lite	I	-	AXI4-Lite Read Address Channel Read Address Valid. • 1 = Read address is valid. • 0 = Read address is not valid.
s_axi_rready	AXI Lite	I	-	AXI4-Lite Read Data Channel Read Data Ready. Indicates target ready to accept the read data. • 1 = Ready to accept data. • 0 = Not ready to accept data.

Signal Name	Interface	Signal Type	Init Status	Description
s_axi_arready	AXI Lite	O	0	AXI4-Lite Read Address Channel Read Address Ready. Indicates DVI ready to accept the read address. • 1 = Ready to accept address. • 0 = Not ready to accept address.
s_axi_rdata (C_S_AXI_DATA_WIDTH-1:0)	AXI Lite	O	zeros	AXI4-Lite Read Data Bus.
s_axi_rresp (1:0)	AXI Lite	O	zeros	AXI4-Lite Read Response Channel Response. Indicates results of the read transfer. The AXI DVI Lite interface always responds with OKAY. • 00b = OKAY - Normal access has been successful. • 01b = EXOKAY - Not supported. • 10b = SLVERR - Not supported. • 11b = DECERR - Not supported.
s_axi_rvalid	AXI Lite	O	0	AXI4-Lite Read Data Channel Read Data Valid. 1 = Read data is valid. 0 = Read data is not valid.
s_axi_wready	AXI Lite	O	0	AXI4-Lite Write Data Channel Write Data Ready. Indicates DVI ready to accept the write data. • 1 = Ready to accept data. • 0 = Not ready to accept data.

Signal Name	Interface	Signal Type	Init Status	Description
s_axi_bresp (1:0)	AXI Lite	O	zeros	AXI4-Lite Write Response Channel. Indicates results of the write transfer. The AXI DVI Lite interface always responds with OKAY. • 00b = OKAY - Normal access has been successful. • 01b = EXOKAY - Not supported. • 10b = SLVERR - Not supported. • 11b = DECERR - Not supported.
s_axi_bvalid	AXI Lite	O	0	AXI4-Lite Write Response Channel Response Valid. Indicates response is valid. • 1 = Response is valid. • 0 = Response is not valid.
s_axi_awready	AXI Lite	O	0	AXI4-Lite Write Address Channel Write Address Ready. Indicates DVI ready to accept the write address. • 1 = Ready to accept address. • 0 = Not ready to accept address.
MM2S Slave Stream Interface Signals				
s_axis_mm2s_aresetn	MM2S	I	-	Primary MM2S Reset In.
s_axis_mm2s_tready	MM2S	O	0	AXI4-Stream Ready. Indicates to master that slave MM2S is ready to receive data. • 1 = Ready to receive data. • 0 = Not ready to receive data.
s_axis_mm2s_tdata (C_AXI_STREAM_DATA_WIDTH-1:0)	MM2S	I	-	AXI4-Stream Data Input.
s_axis_mm2s_tkeep ((C_AXI_STREAM_DATA_WIDTH/8)-1:0)	MM2S	I	-	AXI4-Stream Write Keep. Indicates valid bytes on stream data.

Signal Name	Interface	Signal Type	Init Status	Description
s_axis_mm2s_tlast	MM2S	I	-	AXI4-Stream Last. Indicates last data beat of stream data. • 1 = Last data beat. • 0 = Not last data beat.
s_axis_mm2s_tvalid	MM2S	I	-	AXI4-Stream Valid In. Indicates stream data bus, s_axis_mm2s_tdata, is valid. • 1 = Write data is valid. • 0 = Write data is not valid.
S2MM Master Stream Interface Signals				
m_axis_s2mm_aresetn	S2MM	I	-	Primary S2MM Reset In.
m_axis_s2mm_tvalid	S2MM	O	0	AXI4-Stream Valid Out. Indicates stream data bus, m_axis_s2mm_tdata, is valid • 1 = Write data is valid. • 0 = Write data is not valid.
m_axis_s2mm_tdata (C_AXI_STREAM_DATA_WIDTH-1:0)	S2MM	O	zeros	AXI4-Stream Data Out.
m_axis_s2mm_tkeep ((C_AXI_STREAM_DATA_WIDTH/8)-1:0)	S2MM	O	zeros	AXI4-Stream Write Keep. Indicates valid bytes on stream data.
m_axis_s2mm_tlast	S2MM	O	0	AXI4-Stream Last. Indicates last data beat of stream data. • 1 = Last data beat. • 0 = Not last data beat.
m_axis_s2mm_tready	S2MM	I	-	AXI4-Stream Ready. Indicates to S2MM channel target is ready to receive stream data. • 1 = Ready to receive data. • 0 = Not ready to receive data.
HDMI In Signals				
tmds_rx_clk_p	TMDS_RX	I	-	TMDS Clock+
tmds_rx_clk_n	TMDS_RX	I	-	TMDS Clock-
tmds_rx_2_p	TMDS_RX	I	-	TMDS Data2+
tmds_rx_2_n	TMDS_RX	I	-	TMDS Data2-
tmds_rx_1_p	TMDS_RX	I	-	TMDS Data1+
tmds_rx_1_n	TMDS_RX	I	-	TMDS Data1-
tmds_rx_0_p	TMDS_RX	I	-	TMDS Data0+
tmds_rx_0_n	TMDS_RX	I	-	TMDS Data0-

Signal Name	Interface	Signal Type	Init Status	Description
tmds_rx_scl	TMDS_RX	I	-	TMDS I^2C Serial Clock for DDC.
tmds_rx_sda	TMDS_RX	IO	-	TMDS I^2C Serial Data for DDC.
HDMI Out Signals				
tmds_tx_clk_p	TMDS_TX	O	0	TMDS Clock+
tmds_tx_clk_n	TMDS_TX	O	0	TMDS Clock-
tmds_tx_2_p	TMDS_TX	O	0	TMDS Data2+
tmds_tx_2_n	TMDS_TX	O	0	TMDS Data2-
tmds_tx_1_p	TMDS_TX	O	0	TMDS Data1+
tmds_tx_1_n	TMDS_TX	O	0	TMDS Data1-
tmds_tx_0_p	TMDS_TX	O	0	TMDS Data0+
tmds_tx_0_n	TMDS_TX	O	0	TMDS Data0-

Design Parameters

To allow the user to create the AXI HDMI that is uniquely tailored for the user's system, certain features can be parameterized in the AXI HDMI design. This allows the user to have a design that only utilizes the resources required by the system and operating at the best possible performance. These parameters are show in Table 2.

Table 2. AXI HDMI Parameters

Parameter Name	Allowable Values	Default Values	VHDL Type	Feature/ Description
C_USE_HDMI_RECEIVER	0, 1	1	integer	Include or exclude HDMI Receiver. When excluded, all unused ports are tied off or driven to zero.
C_USE_HDMI_TRANSMITTER	0, 1	1	integer	Include or exclude HDMI Transmitter. When excluded, all unused ports are tied off or driven to zero.
C_USE_HDMI_REGS	0, 1	1	integer	Include or exclude HDMI Software Registers. When excluded, all unused ports are tied off or driven to zero.
C_USE_HDMI_DDC	0, 1	1	integer	Include or

				exclude HDMI Display Data Channel. When excluded, all unused ports are tied off or driven to zero.
AXI4-Lite Slave Interface				
C_S_AXI_DATA_WIDTH	32	32	integer	AXI data bus width.
C_S_AXI_ADDR_WIDTH	32	32	integer	AXI address bus width.
C_S_AXI_MIN_SIZE	0x1FF	0x1FF	std_logic_vector	AXI minimum address space.
C_USE_WSTRB	0	0	integer	AXI include write strobe.
C_DPHASE_TIMEOUT	8	8	integer	AXI delay phase timeout.
C_BASEADDR	Valid Address(1)	0xFFFFFFFF (3)	std_logic_vector	AXI Base Address.
C_HIGHADDR	Valid Address(2)	0x00000000 (3)	std_logic_vector	AXI High Address.
C_FAMILY	virtex6, spartan6	virtex6	string	Target FPGA family.
C_NUM_REG	1	1	integer	AXI number of registers.
C_NUM_MEM	1	1	integer	AXI number of memory spaces.
C_SLV_AWIDTH	32	32	integer	AXI slave address bus width.
C_SLV_DWIDTH	32	32	integer	AXI slave data bus width.

Notes:

1. The user must set the values. The C_BASEADDR must be a multiple of the range, where the range is C_HIGHADDR – C_BASEADDR + 1.
2. C_HIGHADDR – C_BASEADDR must be a power of 2 greater than equal to C_BASEADDR + 0x1FF.
3. An invalid default value will be specified to insure that the actual value is set, i.e. if the value is not set, a compiler error will be generated.

Register Descriptions

Display Resolution

With this register the user can set the desired display resolution, for the HDMI transmitter module. This is a read/write register. If a write request is issued, the user must send the result of the multiplication of the vertical and horizontal size, in pixels, of the desired resolution. By default its value is for 640x480 pixels (0x4B000).

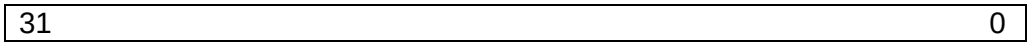


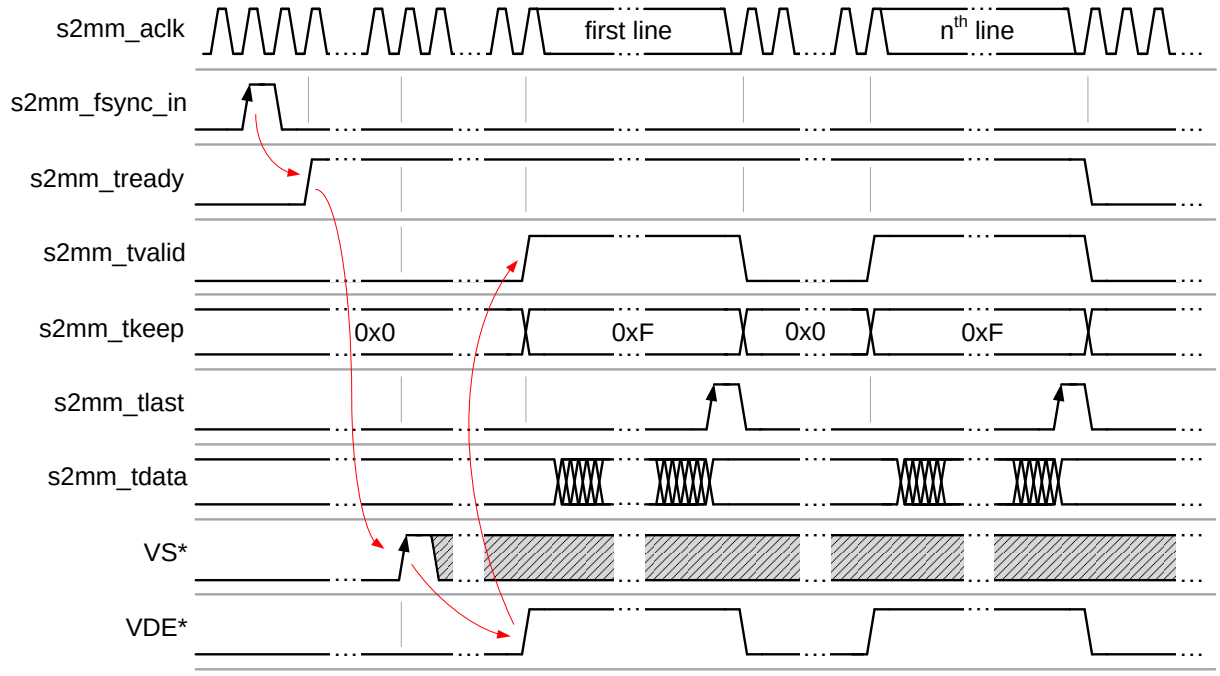
Figure 2. Display Resolution Register

These display resolution values can be:

Table 3. Values of the display resolutions

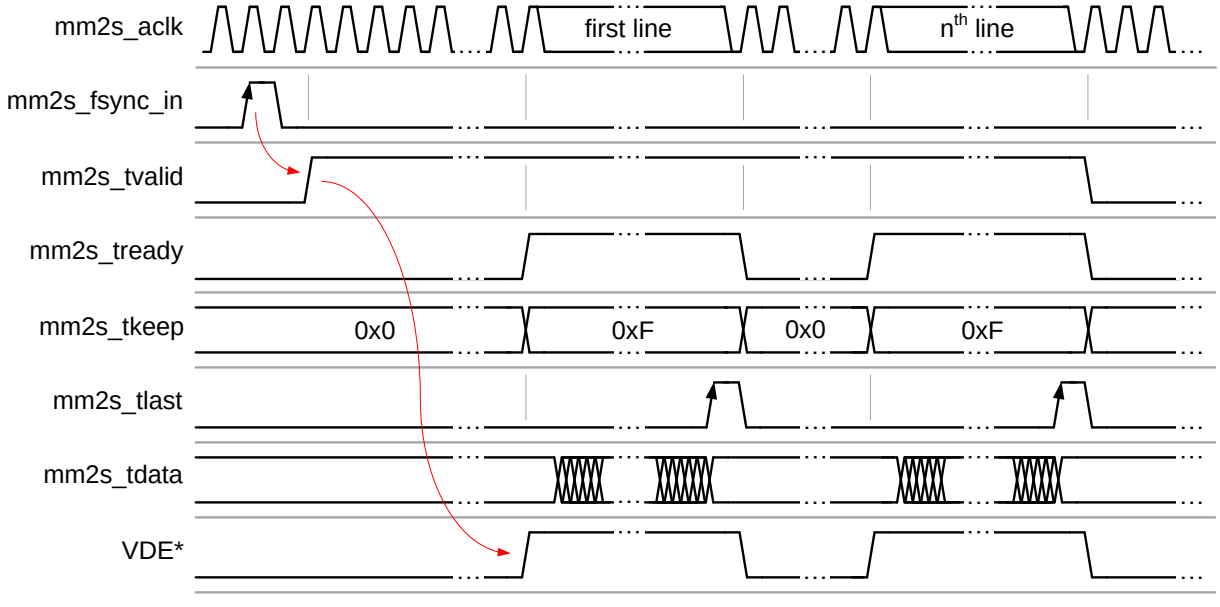
Resolution	Value
640x480	0x4B000
720x480	0x54600
800x600	0x75300
1280x720	0xE1000
1600x900	0x15F900

Timing Diagrams



VS = Internal Vertical Sync pulse
VDE = Video Data Enable

Figure 3. HDMI input start sequence



VDE = Video Data Enable

Figure 4. HDMI output start sequence

References

1. ARM® AMBA® AXI Protocol Version: 2.0 Specification
2. Xilinx Inc., *Spartan-6 Family Overview*: http://www.xilinx.com/support/documentation/data_sheets/ds160.pdf, v2.0, October 25, 2011.
3. Xilinx Inc., *Spartan-6 FPGA Clocking Resources*, v1.6, May 12, 2011.
4. Xilinx Inc., *Implementing a TMDS Video Interface in the Spartan-6 FPGA*: http://www.xilinx.com/support/documentation/application_notes/xapp495_S6TMDS_Video_Interface.pdf, v1.0, December 13, 2010.
5. Xilinx Inc., *LogiCORE IP AXI Video Direct Memory Access*, v4.00.a, October 19, 2011.