PmodCON3™ Reference Component

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Overview

This reference design describes the PmodCON3 VHDL component that will interface with a Digilent PmodCON3 and a Digilent FPGA board. The component generates the pulse width modulated signals to drive the four servos that can be connected to the PmodCON3 according to the inputs.

The component provides the appropriate frequency and modulation.

Features include:

- Takes in four 8-bit vector values for the desired pulse width values for the four channels on the PmodCON3.
- Outputs four pulse width modulated signals at the right frequency to achieve the desired modulation.

Functional Description

Component Architecture

The VHDL component is named CON3RefComp. It has five inputs and four outputs. The input ports are a 50MHz clock and four 8-bit values that represent the desired pulse width values for each of the four channels. The outputs are the four pulse width modulated signals that drive the four servos. A block diagram of the component is shown in Figure 1.

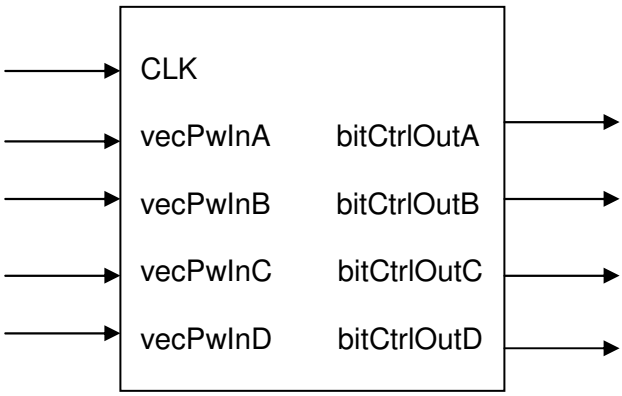


Figure 1 ***The PmodCON3 Reference Component***

Timing

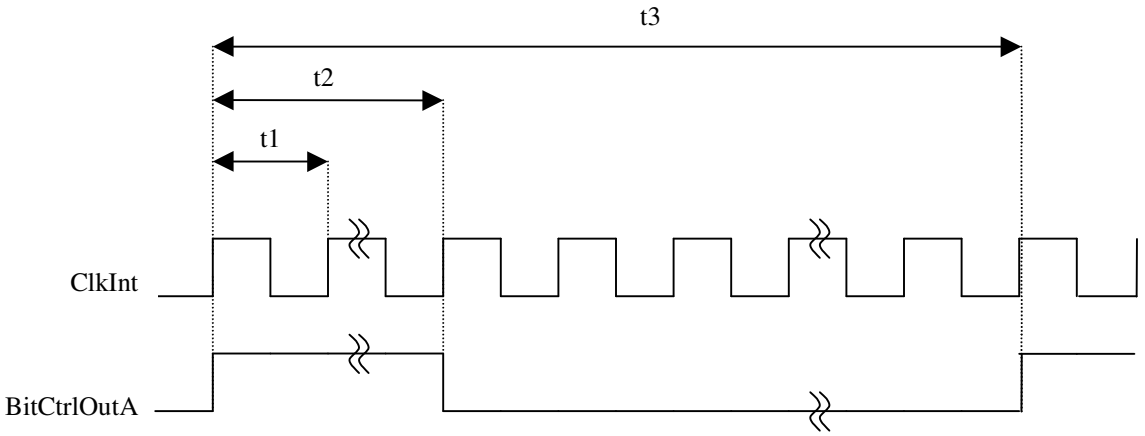
In order to create the pulse width modulated signal for each of the four channels, a divided internal clock (ckInt) running at 50KHz is used. This will provide a resolution of 20µs for the pulse width modulated output signals (bitCtrlOut*).

(The notations bitCtrlOut*, vecPwIn* are used for referring to any of the four postfixed channels A, B, C, or D).

Each of the vecPwIn* input signals specify the number of 20µs ckInt periods that represent the bitCtrlOut* active pulse length. The servos act hazardously with a duty factor of exactly 1 or 0. Therefore, the values (vecPwIn*) are forced on 1 and considered if lower than 255, in order to provide consistent control signals.

In order to accomplish the servos' specifications, the cntPwm counter counts 511 ckInt periods for one bitCtrlOut* period.

The pulse width modulated output signal for channel A (bitCtrlOutA) and the appropriate timings are shown in Figure 2. The timings for all pulse width modulated output signals are similar.



t1 – CkInt period (20 us)
t2 – BitEnOut* active pulse (20us – 20us*255)
t3 – BitEnOut* period (20us*511)

Figure 2 *Pulse Width Modulation*