PmodCLP™ Demo Project

Overview

This document describes the Verilog implementation of the PmodCLP (Character LCD Parallel) demo project for a Nexys3 board. The project is designed in Xilinx ISE Design Suite 14.1. Apart from this documentation, the code uses physical pin names in the Nexys3_Master.ucf to represent the input and output signals. This correspondence is described in the Port Definitions section of this document.

The PmodCLP demo project displays the message "Hello from Digilent" on the first row of the LCD screen when connector J1 of PmodCLP is connected into connector JA of a Nexys3 board and J2 is connected into the lower row of connector JB of a Nexys3 board.

Functional Description

The character LCD allows the user to display character messages on two rows. The PmodCLP receives data or commands through the data bus. The message is written one character at a time. When the message fills the first row it starts shifting left.

The controller sends the *LCD_CMDS_T* array to the LCD. The array contains data and commands. In the array each byte is preceded by two bits. The first bit is used to select between data and instructions registers (*RS*). The second bit is used to select between read and write modes (*RW*). This reference project only writes data to the LCD module. Data can also be read from the LCD, for example, to check when the LCD is busy.

For simplicity, instead of reading back the status of the LCD, a counter (*count*) is used to create the necessary delay for different processes (e.g., 98.3ms is the maximum delay for character writes and shifts; 1.6ms is the delay for clearing the display; 20ms is the delay for powering on, etc.) The state machine moves from one state to another only after the minimum delay period for the previous operation has passed.

The RS signal (Register Selection) is used to select between the data register and the instruction register. To select the data register, RS must be set high; to select the instruction register, RS must be set low.

The RW signal (Read / Write) is used to select between read and write mode. To select the read mode, RW must be set high; to select the write mode, RW must be set low.

The E signal (Enable) is used to start reading / writing the data.

The Character LCD Component needs a 100MHz clock on the clk input.
When activated the rst (reset) input signal restarts the controller from the initial state.
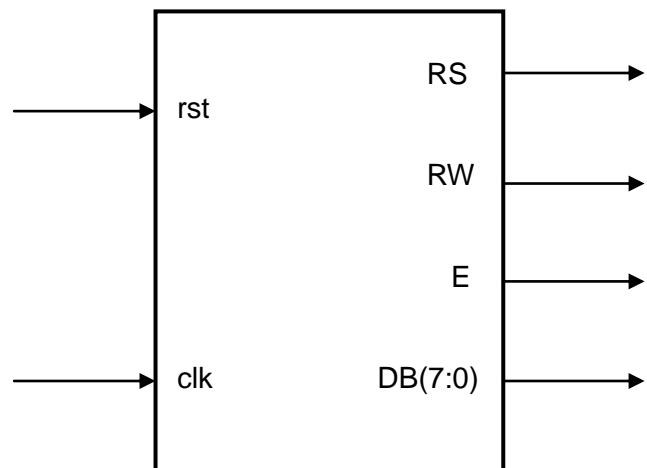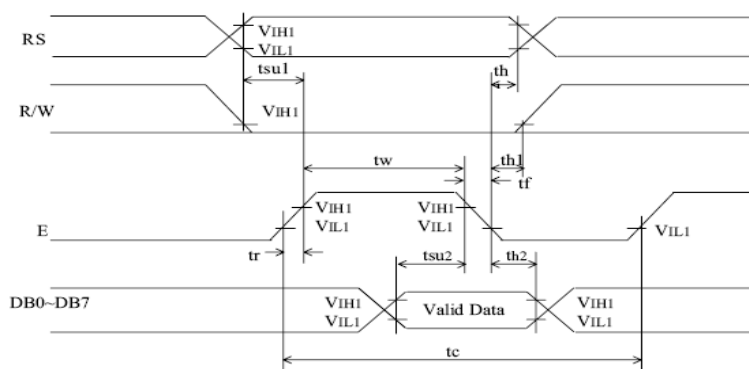

Figure 1 *Character LCD Reference Project*

Port Definitions

Signal Name	Pin Name	Definitions
rst	BTN(3)	input pin, global reset signal
clk	clk	input pin, clock signal that has a 100MHz frequency
RS	JB(4)	output pin, register selection
RW	JB(5)	output pin, read/write used to select between read and write mode
E	JB(6)	output pin, start enable signal to read or write data
DB(7:0)	JA(7:0)	output bus, eight data bus lines used for data transfer

Write Cycle Example

• Write cycle

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Pin
Enable cycle time	tc	500	-	-	ns	E
Enable "H" level pulse width	tw	220	-	-	ns	E
Enable rise /fall time	tr,tf	-	-	25	ns	E
RS,R/W setup time	tsu	40	-	-	ns	RS,R/W
RS,R/W address hold time	th	10	-	-	ns	RS,R/W
Read data output delay time	tD	60	-	-	ns	DB0~DB7
Read data hold time	tDH	10	-	-	ns	DB0~DB7

To write data in the data register of the LCD:
- The R/W signal must be set low.
- The RS signal must be set high.
- DB0-DB7 must contain valid data.
- E must be asserted high for at least 220ns and asserted low after that. The minimum enable cycle time is 500*ns.*