PmodPS/2™ Demo Project

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Overview

This document describes a Verilog demo project that interfaces with a PmodPS/2. The project was developed on a Spartan-6 based Nexys3 board in Xilinx ISE Design Suite 14.2, but it is easily retargeted to any other FPGA.

This demo allows a PS/2 mouse to control a cursor on a VGA monitor via the PmodPS/2. The resolution to the monitor may be switched between 800x600 and 640x480. The PmodPS/2 is connected to the lower row of the JA Pmod connector on the Nexys3.

Functional Description

In addition to the components developed for this project, there are several Digilent reference components instantiated. They are: MouseRefComp, VgaRefComp, and mouse_displayer. For details about these components, please see their respective reference documents and the source file comments.

The system initially uses the dcm_all component and the 100 MHz core clock to produce 25 MHz and 40 MHz clock signals. The 25 MHz signal is used to time the 640x480 VGA display, and the 40 MHz signal is used to time the 800x600 VGA display. Both clock signals are sent to the VgaRefComp component; however a BUFGMUX must be used to select which clock is sent to the MouseRefComp component. Control for this multiplexor is tied directly to SW0 on the Nexys3.

The MouseRefComp communicates through the PS/2 interface and initialized at power-up or reset. After initializing the mouse, the component outputs the current state of the Left, Middle, and Right mouse buttons along with the position along the X and Y axis. A Z axis position may also be used to report the position of the scroll wheel if present. The left, middle, and right mouse buttons are tied directly to LED 2, 1, and 0 respectively on the Nexys3 board so that when a button is pressed, the LED is activated.

The X and Y position signals are routed to the mouse_displayer reference component. This component takes information about the position of the mouse along with data from the VgaRefComp on the background image and the vertical and horizontal pixel position. This data is used to generate the 8-bit VGA color data (3-bit red, 3-bit green, 2-bit blue) needed to overlay the cursor on the original image. The color data is driven directly to the VGA port pins on the Nexys3. In this project, the inputs for the background image are unconnected, and so the background image is black.

In addition to the above functionality, the BTNL and BTNR momentary switches are used to reset the cursor to the center of the screen and to reset the VGA display, respectively.

Block Description

Digital Clock Manager (dcm_all.vhd):

This component takes input from the 100 MHz oscillator on the Nexys3 and produces two additional clock signals for use in the demo. One of the output signals is a 25 MHz clock and the other is a 40 MHz clock. This block was generated using an IP CORE in Xilinx 14.2, from which the HDL Functional Model was extracted. The Digital Clock Manager uses one of the four physical DCMs on the Spartan-6 LX16 FPGA to operate.

Mouse Reference Component (MouseRefComp.vhd):

This component is used to keep track of the current state of the mouse including position and button presses, as well as the expected resolution for boundaries on mouse movement. It also prepares and maintains the PS/2 interface. The component contains three blocks: The resolution_mouse_informer, the mouse_controller, and the ps2interface. Descriptions of the functionality of these blocks may be found in the MouseRefComp reference manual on the Digilent Inc. website.

VGA Reference Component (VgaRefComp.vhd):

This component is used to drive the VGA display's H-Sync and V-Sync signals along with the blanking signals. The component contains three blocks, two of which are resolution controllers for 640x480 and 800x600 operations. The third block is a VGA selector which is used to determine which of the two resolutions should be output to the screen. Further information on the VgaRefComp may be found in its reference manual on the Digilent Inc. website.

Mouse Displayer (mouse_displayer.vhd):

This component takes input from the MouseRefComp and VgaRefComp to overlay the mouse cursor over the image on the display. Details about its operation may be found on the Digilent Inc. website.

Setup and Operation of the Demo

The demo requires that the user attach the PmodPS/2 to the lower row of the JA Pmod connector on the Nexus3. A VGA cable should be connected from the VGA output on the Nexys3 to a VGA compatible monitor. After loading the .bit file to the FPGA. The cursor may be moved on screen by moving the attached mouse. Left clicking will illuminate LD2, middle clicking will illuminate LD1, and right clicking will illuminate LD0. The resolution may be switched from 640x480 to 800x600 by moving SW0 to its ON position. It may be switched back by moving the switch to the off position. The VGA display may be reset by pressing BTNR and the cursor may be reset to the center of the screen by pressing BTNL.