

System Board
RA Male

- 1 IDI
- 2 IDO
- 3 TMS
- 4 TCK
- 5 M-INT
- 6 ITSEI
- 7 M-WAIT
- 8 M-RESET
- 9 M-DSTB
- 10 M-WRITE
- 11 M-DB7
- 12 M-ASTB
- 13 M-DB5
- 14 M-DB6
- 15 M-DB3
- 16 M-DB4
- 17 M-DB1
- 18 M-DB2
- 19 L SBCLK
- 20 M-DB0
- 21 DB7
- 22 CS
- 23 DB6
- 24 OF
- 25 DB5
- 26 WF
- 27 DB4
- 28 ADR5
- 29 DB3
- 30 ADR4
- 31 DB2
- 32 ADR3
- 33 DB1
- 34 ADR2
- 35 DB0
- 36 ADR1
- 37 UCC33
- 38 ADR0
- 39 GND
- 40 VU

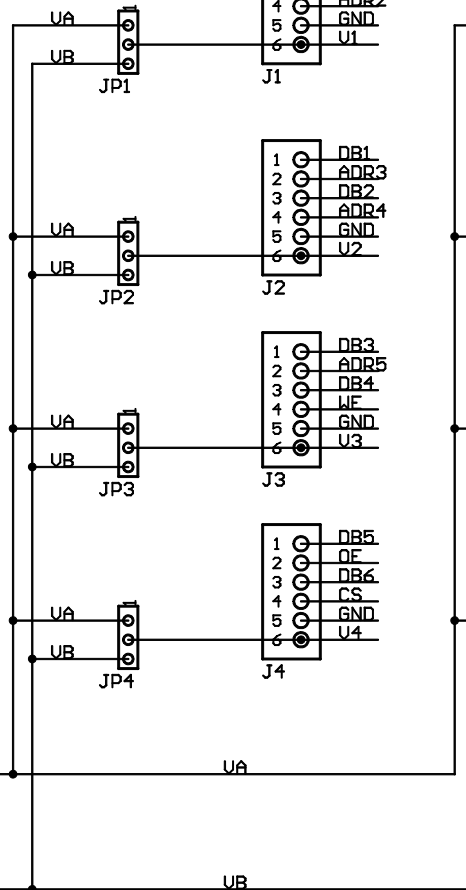
J10

- 1 UF
- 2 GND

J9

- 1 VU
- 2 UCC33
- 3 UF

JP10



Peripheral Board
RA Female

- 1 GND
- 2 VU
- 3 UCC33
- 4 ADR0
- 5 DB0
- 6 ADR1
- 7 DB1
- 8 ADR2
- 9 DB2
- 10 ADR3
- 11 DB3
- 12 ADR4
- 13 DB4
- 14 ADR5
- 15 DB5
- 16 WF
- 17 DB6
- 18 OF
- 19 DB7
- 20 CS
- 21 L SBCLK
- 22 M-DB0
- 23 M-DB1
- 24 M-DB2
- 25 M-DB3
- 26 M-DB4
- 27 M-DB5
- 28 M-DB6
- 29 M-DB7
- 30 M-ASTB
- 31 M-DSTB
- 32 M-WRITE
- 33 M-WAIT
- 34 M-RESET
- 35 M-INT
- 36 ITSEI
- 37 TMS
- 38 TCK
- 39 TDI
- 40 TDO

J11

- 1 DB7
- 2 M-DB0
- 3 L SBCLK
- 4 M-DB2
- 5 GND
- 6 U5

J5

- 1 M-DB1
- 2 M-DB4
- 3 M-DB3
- 4 M-DB6
- 5 GND
- 6 U6

J6

- 1 M-DB5
- 2 M-ASTB
- 3 M-DB7
- 4 M-WRITE
- 5 GND
- 6 U7

J7

- 1 M-DSTB
- 2 M-RESET
- 3 M-WAIT
- 4 M-INT
- 5 GND
- 6 U8

J8

Digilent Module Interface Board		Engineer: NEA
Copyright 2004		Author: GMA
TITLE: MIB		Rev: B
Document Number: 500-057		Sheet: 1/1
Release Date: 8/19/2004		