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Sync 1.0 IP Core User Guide

Revised October 30, 2015; Author Elod Gyorgy

1 Introduction

This user guide describes the Digilent Sync Intellectual Property. This IP provides clock domain crossing for signals where variable crossing latency does not affect functionality.

IP quick facts	
Supported device families	Zynq®-7000, 7 series
Supported user interfaces	N/A
Provided with core	
Design files	VHDL
Simulation model	VHDL Behavioral
Constraints file	XDC
Software driver	N/A
Tested design flows	
Design entry	Vivado™ Design Suite 2015.3
Synthesis	Vivado Synthesis 2015.3

2 Features

- Brings global reset into a local clock domain where reset has to be synchronously de-asserted
- Brings asynchronous signal into a synchronous domain

3 Performance

No clock constraints are defined in this IP. Maximum frequency depends on the switching performance of flip-flops and the IP should not be the limiting factor in timing closure.

The IP properly defines false path constraints between source and destination clock domains.

4 Use cases

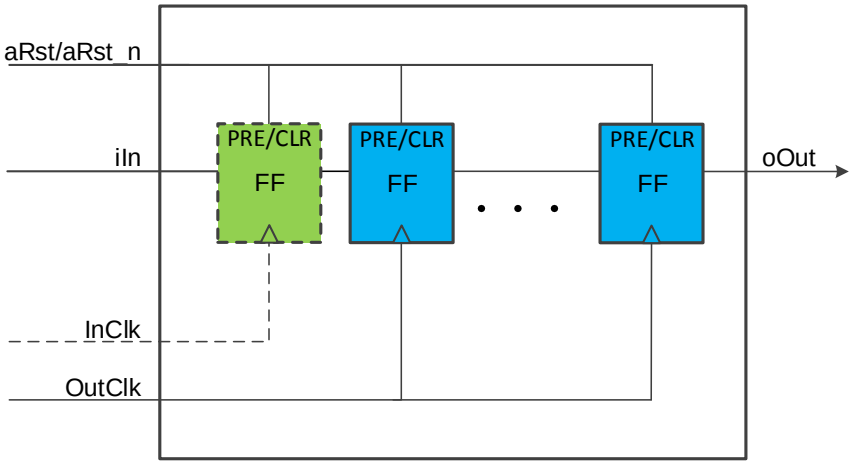

Figure 1. Sync internal diagram

The IP instantiates flip-flops and forms a chain that passes the input signal (iIn) towards the output (oOut). The first flip-flop is optional and works on the input (source) clock domain. It re-registers the input to make sure the downstream synchronizer chain has a glitch-free input. All the other flip-flops work on the output (destination) clock domain and each lowers the chance of failure due to metastability by increasing the time available for these events to settle. The number of synchronizer stages can be customized in the IP configuration wizard.

4.1 Local reset

Consider a global reset signal that is asynchronous to a local clock domain you wish to reset. Depending on the application it might be important to de-assert the reset synchronous to the local clock, so that it can be guaranteed that all circuits come out of reset simultaneously. Reset assertion remains asynchronous, which is useful in cases where the local clock can be stopped.

Specify the correct polarity for the input reset signal in IP configuration and tie it to the aRst or aRst_n pin. Configure the output reset value to 0 or 1, depending on the desired polarity of the output reset signal. The input pin iIn should be tied to the constant inactive value of the output reset. Re-registering iIn is not required in this use case.

4.2 Asynchronous input

Any input signal asynchronous to circuits it is connected to has the chance to become metastable. Using synchronizers lowers the chance of failure significantly. If the source clock of the input is known (synchronous to a known clock domain), tick “Re-register input on its source domain” and connect the source clock to InClk. If the source clock is not available, disable this option. Connecting a reset is optional and can be left unconnected.

5 Port Descriptions

Signal Name	Interface	Signal Type	Init State	Description
aRst(_n)	-	I	N/A	Asynchronous reset of configurable polarity. Optional
InClk	-	I	N/A	Source clock for iIn. Optional
OutClk	-	I	N/A	Destination clock for oOut.
iIn	-	I	N/A	Input signal to be synchronized.
oOut	-	O	configurable	Input iIn synchronized to OutClk.

Table 1. Port descriptions.

6 Designing with the core

6.1 Customization

The IP provides four customizable parameters: the polarity of reset signal, the reset value of oOut, option to re-register iIn, and the number of synchronizer stages to use.