Digilent D2-FT System Board Reference Manual

December 6, 2004

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Overview

The Digilent D2-FT circuit board provides the basis for a complete circuit development platform centered on a Xilinx Spartan 2E FPGA. D2-FT features include:

- A Xilinx XC2S300E FPGA with 300K gates and 350MHz operation (also available with the XC2S400E FPGA);
- 172 user I/Os routed to six standard 40-pin expansion connectors;
- A socket for a JTAG-programmable 18V02 configuration Flash ROM;
- Dual on-board 1.5A power regulators (1.8V and 3.3V);
- An SMD 50MHz oscillator, and a socket for a second oscillator;
- A JTAG programming port;
- A status LED and pushbutton for basic I/O.

The D2-FT has been designed to work with all versions of the Xilinx ISE CAD tools, including the free WebPack tools available at Xilinx web site. (www.xilinx.com) A growing collection of low-cost expansion boards can be used with the D2-FT to add analog and digital I/O capabilities, as well as various data ports like Ethernet and USB. The D2-FT board ships with a power supply and programming cable, so designs can be implemented immediately without the need for any additional hardware.

Functional Description

The Digilab D2-FT provides a minimal system that can be used to rapidly implement FPGA-based circuits, or to gain exposure to Xilinx CAD tools and Spartan 2E devices. The D2-FT provides only the essential supporting devices for the Spartan 2E FPGA, including clock sources and power supplies. All available I/O signals are routed to standard expansion

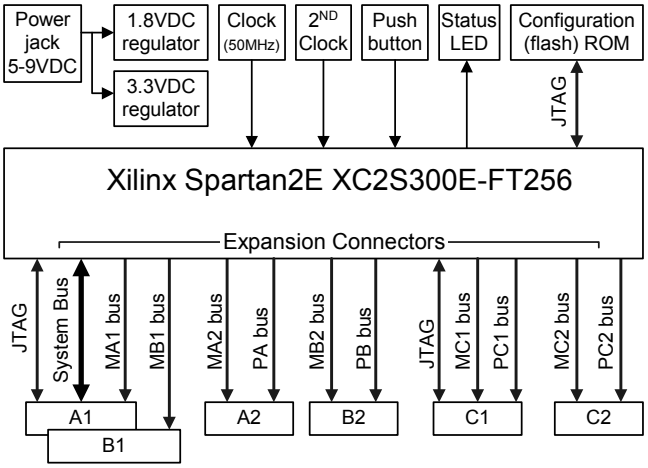

Figure 1. D2-FT Circuit Board Block Diagram

connectors that mate with 40-pin, 100 mil spaced DIP headers available from any catalog distributor. A pushbutton and LED are also included for basic I/O.

The D2-FT board has been designed to serve primarily as a host for peripheral boards. Each of the six expansion connectors provides the unregulated supply voltage (VU), 3.3V, GND, and 32 I/O signals from the FPGA. Because there are more connector pins than FPGA pins, the A1 and B1 connectors share an 18-pin bus. All other connector positions are driven by individual FPGA signals. JTAG signals are also routed to the A1, B1, and C1 expansion connectors. This allows peripheral boards to drive the scan chain, or to be configured along with the Spartan 2E FPGA.

Application-specific peripheral boards can be created to mate with the D2-FT, or ready-made peripheral boards that offer many standard I/O and data port functions can be obtained from Digilent (for a current listing of available boards, see www.digilentinc.com).

JTAG Scan Chain and Device Configuration

The Spartan 2E FPGA, the 18V00 ROM on the D2-FT, and any programmable devices on peripheral boards attached to the D2-FT can be programmed via their JTAG ports. The JTAG scan chain is routed to the FPGA, the ROM, and around the board to four connection ports as shown in Figure 2 below. The primary configuration port (Port 1) uses a standard 6-pin JTAG header (J7) that can accommodate Digilent's JTAG3 cable (or cables from Xilinx or other vendors). The other three JTAG programming ports are bi-directional, and they are available on the A1, B1, and C1 expansion connectors. If no peripheral board is present, a buffer on the D2-FT removes the expansion connector from the JTAG chain. If a peripheral board with a JTAG device is attached, the scan chain is driven out the expansion connector so that any JTAG-programmable parts can be configured. If a Digilent port module is connected to one of the three JTAG-enabled expansion connectors, then the port module can drive the JTAG chain to program all devices in the scan chain (port modules include Ethernet, USB, EPP parallel, and serial modules -- see www.digilentinc.com for more information).

The scan chain can be driven from the primary port by powering on the D2-FT, connecting it to a PC with a JTAG programming cable, and running the "auto-detect" feature of the configuration software. The configuration software allows devices in the scan chain to be selectively programmed with any available configuration file. If no programming ROM is loaded in the IC5 socket (or if ROM is present but is not to be included in the scan chain), jumper-shunts must be loaded at JP1 and JP2 in the "Bypass ROM" location to route the JTAG chain around the ROM socket. If an 18V02 (or larger) ROM is loaded in the IC5 socket, it can be included in the scan chain by loading the JP1 and JP2 jumper-shunts in the "Include ROM" positions.

If a programming ROM is present in the IC5 socket, the FPGA will automatically access the ROM for configuration data if jumper shunts are loaded in all three positions of J8 (M2, M1, and M0).

Port modules attached to ports A1, B1, or C1 can drive the scan chain if a jumper-shunt is installed on the primary JTAG header across the TDI and TDO pins. In their default state, Digilent port modules will appear as a JTAG cable to the configuration software. Port modules can disable their JTAG drivers; if more than one JTAG driver is enabled on the scan chain, programming may fail.

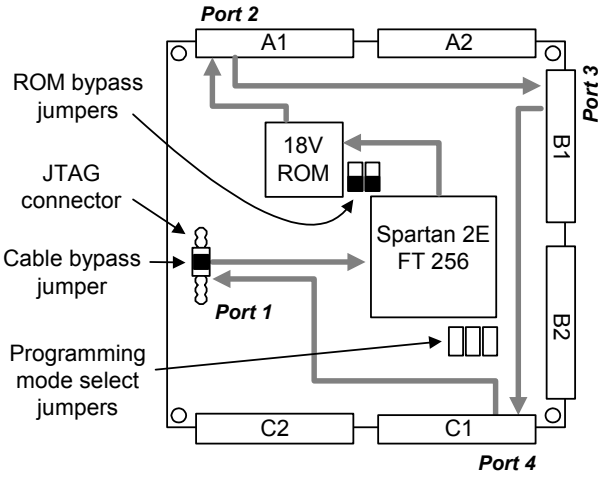

Figure 2. JTAG Signal Routing on D2-FT

Power Supplies

The D2-FT board uses two LM317 voltage regulators to produce a 1.8VDC supply for the Spartan 2E core, and 3.3VDC supply for the I/O ring. Both regulators have good bypass capacitance, allowing them to supply up to 1.5A of current with less than 50mV of noise (typical). Power can be supplied from a low-cost wall transformer supply. The external supply must use a 2.1mm center-positive connector, and it must produce between 6VDC and 12VDC of unregulated voltage.

The D2-FT uses a four layer PCB, with the inner layers dedicated to VCC and GND planes. Most of the VCC plane is at 3.3V, with an island under the FPGA at 1.8V. The FPGA and the other ICs on the board all have 0.047uF bypass capacitors placed as close as possible to each VCC pin.

Total board current is dependant on FPGA configuration, clock frequency, and external connections. In test circuits with roughly 50K gates routed, a 50MHz clock source, and a single expansion board attached (the DIO5 board), approximately 200mA +/- 30% of supply current is drawn from the 1.8V supply, and approximately 200mA +/- 50% is drawn from the 3.3V supply. These currents are strongly dependent on FPGA and peripheral board configurations.

All FPGA I/O signals use the VCCO voltage derived from the 3.3V supply. If other VCCO voltages are required, the regulator output can be modified by changing R12 according to:

VCCO = 1.25(1 + R12/R11).

Refer to the LM317 data sheet and D2-FT schematic for further information.

Oscillators

The D2-FT provides a 50MHz SMD primary oscillator and a socket for a second oscillator. The primary oscillator is connected to the GLK2 input of the Spartan 2E (pin B8), and the secondary oscillator is connected to GCLK3 (pin C8). Both clock inputs can drive the DLL on the Spartan 2E, allowing for internal frequencies up to four times higher than the external clock signals. Any 3.3V oscillator in a half-size DIP package can be loaded into the secondary oscillator socket.

Pushbutton and LED

A single pushbutton and LED are provided on the board allowing basic status and control functions to be implemented without a peripheral board. As examples, the LED can be illuminated from a signal in the FPGA to verify that configuration has been successful, and the pushbutton can be used to provide a basic reset function independent of other inputs. The circuits are shown in Figure 3.

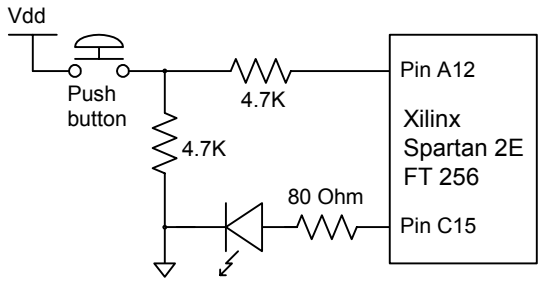

Figure 3. LED and Pushbutton Circuit

Expansion Connectors

The six expansion connectors labeled A1-A2, B1-B2, and C1-C2 use 2x20 right-angle headers with100 mil spacing. All six connectors have GND on pin 1, VU on pin 2, and 3.3V on pin 3. Pins 4-35 route to FPGA I/O signals, and pins 36-40 are reserved for JTAG and/or clock signals. (See Figure 4)

The expansion headers provide 192 signal connections, and the Spartan 2E-FT256 has 172 available I/O signals. Thus, some FPGA signals are routed to more than one connector. The lower 18 pins (pins 4-21) of the A1and B1 connectors are connected to the same 18 FPGA pins, and they are designated as the "system bus" (a unique chip select signal is routed to each connector). Other than these 18 shared signals, all remaining FPGA signals are routed to individual expansion connector positions.

The lower 18 pins of the A2, B2, and C2 connectors are designated as "peripheral busses", and each of these busses (named PA, PB, and PC) use 18 unique signals. The 14 upper pins of each expansion connector (pins 22-35) have been designated as "module busses". Each connector has a fully populated module bus (named MA1, MA2, MB1, MB2, MC1, and MC2).

System Bus

The "system bus" is a protocol used by certain expansion boards that mimics a simple 8-bit microprocessor bus. It uses eight data lines, six address lines, a write-enable (WE) strobe that can be used by the peripheral to latch

written data, an output-enable (OE) strobe that can be used by the peripheral to enable read data, a chip select, and a clock to enable synchronous transfers. System bus timings can be used to configure the lower 18 pins of the A1, B1, and C1 connectors (the lower 18 pins of A1 and B1 share the same FPGA pins). The diagrams below show signal timings assumed by Digilent to create peripheral devices. However, any bus and timing models can be used by modifying circuits in the FPGA and attached peripheral devices.

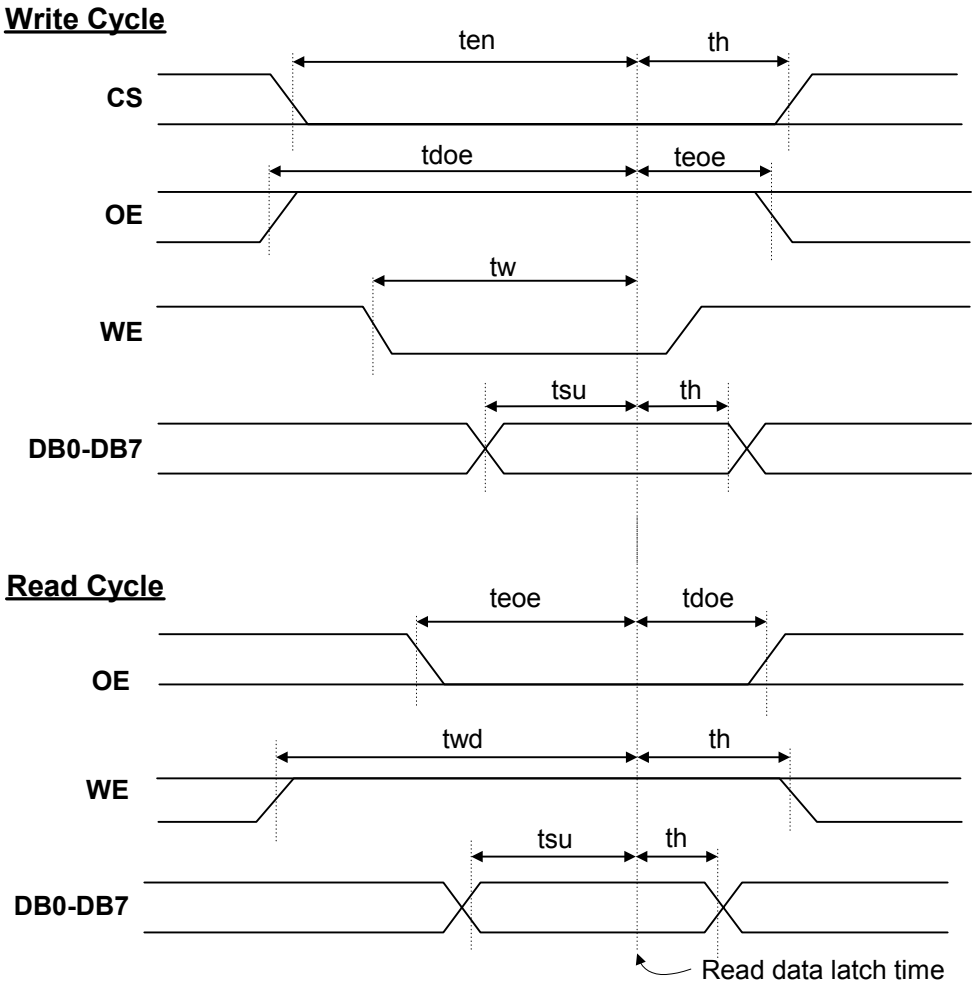

Figure 4. System Bus Timing

Table 1. System Bus Timing		
Symbol	**Parameter**	**Time (typ)**
ten	Time to enable after CS asserted	10ns
th	Hold time	1ns
tdoe	Time to disable after OE de-asserted	10ns
teoe	Time to enable after OE asserted	15ns
tw	Write strobe time	10ns
tsu	Data setup time	5ns
twd	Write disable time	0ns

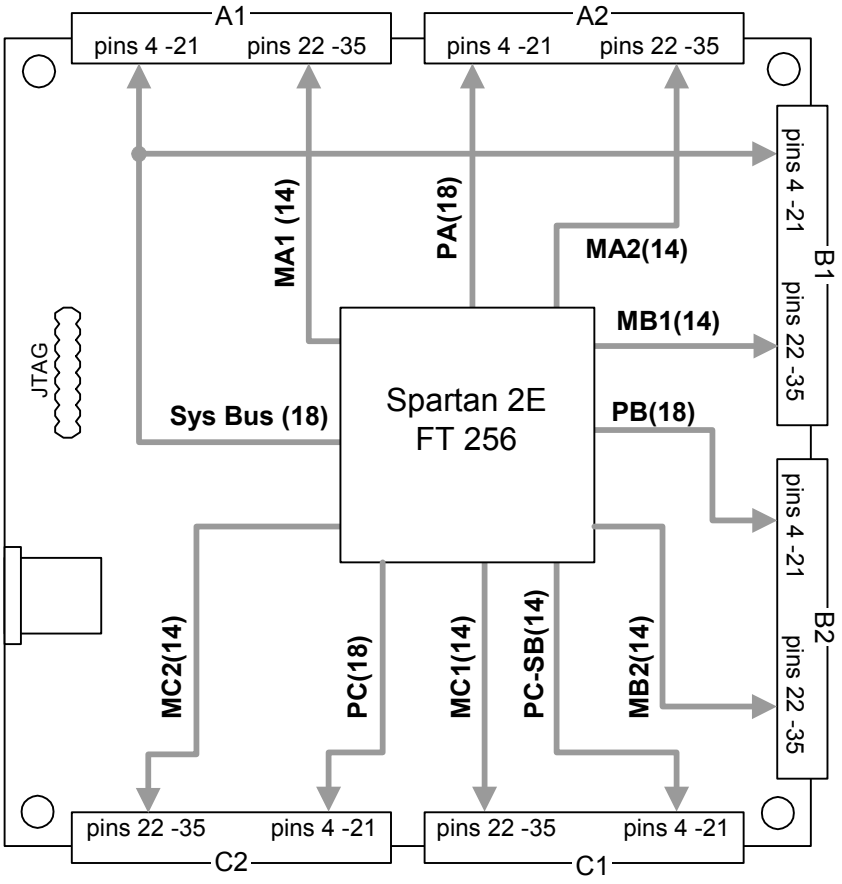

Figure 5. Expansion Connector Signal Routing

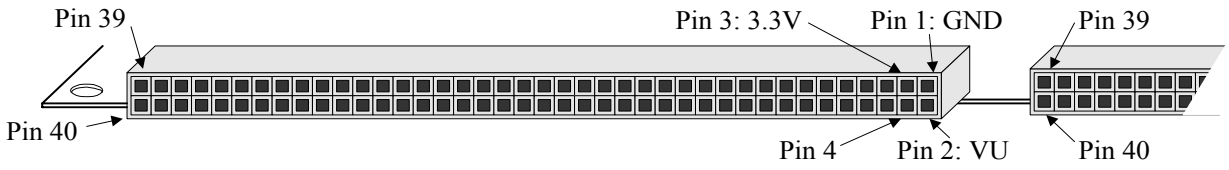

Figure 6. Expansion Connector Pin Locations

Table 2. D2-FT Expansion Connector Pinout												
Pin #	A1		A2		B1		B2		C1		C2	
	Signal	FPGA Pin	Signal	FPGA Pin	Signal	FPGA Pin	Signal	FPGA Pin	Signal	FPGA Pin	Signal	FPGA Pin
1	GND		GND		GND		GND		GND		GND	
2	VU		VU		VU		VU		VU		VU	
3	VCC33		VCC33		VCC33		VCC33		VCC33		VCC33	
4	ADR0	J14	PAI01	B12	ADR0	J14	PBI01	M10	PCADR0	N3	PCI01	F2
5	DB0	K16	PAI02	C12	DB0	K16	PBI02	R11	PCDB0	P2	PCI02	E1
6	ADR1	K13	PAI03	A13	ADR1	K13	PBI03	P10	PCADR1	L5	PCI03	F4
7	DB1	K15	PAI04	D12	DB1	K15	PBI04	T10	PCDB1	N1	PCI04	E2
8	ADR2	K14	PAI05	B13	ADR2	K14	PBI05	N10	PCADR2	M3	PCI05	E3
9	DB2	L16	PAI06	A14	DB2	L16	PBI06	P9	PCDB2	N2	PCI06	D1
10	ADR3	K12	PAI07	E11	ADR3	K12	PBI07	R10	PCADR3	L4	PCI07	F5
11	DB3	L15	PAIO8	C16	DB3	L15	PBI08	N9	PCDB3	M1	PCI08	D2
12	ADR4	L14	PAI09	E13	ADR4	L14	PBI09	N8	PCADR4	L3	PCI09	D3
13	DB4	M16	PAI010	D14	DB4	M16	PBI010	R9	PCDB4	M2	PCI010	C1
14	ADR5	L13	PAI011	D16	ADR5	L13	PBI011	P8	PCADR5	K5	PCI011	E4
15	DB5	M15	PAI012	F12	DB5	M15	PBI012	R8	PCDB5	L1	PCI012	A3
16	WE	M14	PAI013	D15	WE	M14	PBI013	N7	PCWE	K3	PCI013	C2
17	DB6	N16	PAI014	E14	DB6	N16	PBI014	T7	PCDB6	L2	PCI014	B3
18	OE	L12	PAI015	E16	OE	L12	PBI015	P7	PCOE	K4	PCI015	C4
19	DB7	N15	PAI016	F13	DB7	N15	PBI016	R7	PCDB7	K1	PCI016	A4
20	CSA	D8	PAI017	E15	CSB	N14	PBI017	M7	PCCS	J3	PCI017	DS
21	LSBCLK	P16	PAI018	F14	LSBCLK	P16	PBI018	T6	PCCLK	K2	PCI018	B4
22	MA1DB0	D9	MA2DB0	F16	MB1DB0	M13	MB2DB0	P6	MC1DB0	J4	MC2DB0	C5
23	MA1DB1	A9	MA2DB1	G12	MB1DB1	T14	MB2DB1	R6	MC1DB1	J1	MC2DB1	A5
24	MA1DB2	C9	MA2DB2	F15	MB1DB2	N12	MB2DB2	N6	MC1DB2	J2	MC2DB2	E6
25	MA1DB3	B9	MA2DB3	G14	MB1DB3	R14	MB2DB3	T5	MC1DB3	H4	MC2DB3	B5
26	MA1DB4	D10	MA2DB4	G16	MB1DB4	P13	MB2DB4	P5	MC1DB4	H1	MC2DB4	C6
27	MA1DB5	A10	MA2DB5	G13	MB1DB5	T13	MB2DB5	R5	MC1DB5	H3	MC2DB5	A6
28	MA1DB6	C10	MA2DB6	G15	MB1DB6	M11	MB2DB6	M6	MC1DB6	H2	MC2DB6	D6
29	MA1DB7	B10	MA2DB7	H14	MB1DB7	R13	MB2DB7	T4	MC1DB7	G4	MC2DB7	B6
30	MA1ASTB	E10	MA2ASTB	H16	MB1AST	P12	MB2AST	P4	MC1ASTB	G1	MC2ASTB	C7
31	MA1DSTB	A11	MA2DSTB	H13	MB1DST	T12	MB2DST	R4	MC1DSTB	G3	MC2DSTB	A7
32	MA1WRT	C11	MA2WRT	H15	MB1WRT	N11	MB2WRT	N5	MC1WRT	G2	MC2WRT	D7
33	MA1WAIT	B11	MA2WAIT	J16	MB1WAIT	R12	MB2WAIT	T3	MC1WAIT	G5	MC2WAIT	E7
34	MA1RST	D11	MA2RST	J13	MB1RST	P11	MB2RST	M4	MC1RST	F1	MC2RST	B7
35	MA1INT	A12	MA2INT	J15	MB1INT	T11	MB2INT	P1	MC1INT	F3	MC2INT	A8
36	JTSELA				JTSELB				JTSELC			
37	TMS				TMS				TMS			
38	TCK				TCK				TCK			
39	TDOA		CLK0	T9	TDOB				TDOC		CLK1	T8
40	TDIA		GND		TDIB				TDIC		GND	

Table 3. D2-FT FPGA Pin Assignments

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T
1	**GND**	*TMS*	PC-IO10	PC-IO6	PC-IO2	PC-RST	MC1-ASTB	MC1-DB4	MC1-DB1	PC-DB7	PC-DB5	PC-DB3	PC-DB1	MB2-INT	*M1*	**GND**
2	*TCK*	**GND**	PC-IO13	PC-IO8	PC-IO4	PC-IO1	MC1-WRT	MC1-DB6	MC1-DB2	PC-CLK	PC-DB6	PC-DB4	PC-DB2	PC-DB0	**GND**	*M0*
3	PC-IO12	PC-IO14	**VCCI**	PC-IO9	PC-IO5	MC1-INT	MC1-DSTB	MC1-DB5	MC1-CS	PC-WE	PC-ADR4	PC-ADR2	PC-ADR0	**VCCI**	*M2*	MB2-WAIT
4	PC-IO16	PC-IO18	PC-IO15	**VCCI**	PC-IO11	PC-IO3	MC1-DB7	MC1-DB3	MC1-D80	PC-OE	PC-ADR3	MB2-RST	**VCCI**	MB2-ASTB	MB2-DSTB	MB2-DB7
5	MC2-DB1	MC2-DB3	MC2-DB0	PC-IO17	**VCCI**	PC-IO7	MC1-WAIT	**VCCO**	**VCCO**	PC-ADR5	PC-ADR1	**VCCI**	MB2-WRT	MB2-DB4	MB2-DB5	MB2-DB3
6	MC2-DB5	MC2-DB7	MC2-DB4	MC2-DB6	MC2-DB2	**GND**	**VCCO**	**VCCO**	**VCCO**	**VCCO**	**GND**	MB2-DB6	MB2-DB2	MB2-DB0	MB2-DB1	PB-IO18
7	MC2-DSTB	MC2-RST	MC2-ASTB	MC2-WRT	MC2-WAIT	**VCCO**	**GND**	**GND**	**GND**	**GND**	**VCCO**	PB-IO17	PB-IO13	PB-IO15	PB-IO16	PB-IO14
8	MC2-INT	**GCK2**	**GCK3**	CSA	**VCCO**	**VCCO**	**GND**	**GND**	**GND**	**GND**	**VCCO**	**VCCO**	PB-IO9	PB-IO11	PB-IO12	GCK1
9	MA1-DB1	MA1-DB3	MA1-DB2	MA1-DB0	**VCCO**	**VCCO**	**GND**	**GND**	**GND**	**GND**	**VCCO**	**VCCO**	PB-IO8	PB-IO6	PB-IO10	GCK0
10	MA1-DB5	MA1-DB7	MA1-DB6	MA1-DB4	MA1-ASTB	**VCCO**	**GND**	**GND**	**GND**	**GND**	**VCCO**	PB-IO1	PB-IO5	PB-IO3	PB-IO7	PB-IO4
11	MA1-DSTB	MA1-WAIT	MA1-WRT	MA1-RST	PA-IO7	**GND**	**VCCO**	**VCCO**	**VCCO**	**VCCO**	**GND**	MB1-DB6	MB1-WRT	MB1-RST	PB-IO2	MB1-INT
12	MA1-INT **BTN**	PA-IO1	PA-IO2	PA-IO4	**VCCI**	PA-IO12	MA2-DB1	**VCCO**	**VCCO**	ADR3	OE	**VCCI**	MB1-DB2	MB1-ASTB	MB1-WAIT	MB1-DSTB
13	PA-IO3	PA-IO5	*TDI*	**VCCI**	PA-IO9	PA-IO16	MA2-DB5	MA2-DSTB	MA2-RST	ADR1	ADR5	MB1-DB0	**VCCI**	MB1-DB4	MB1-DB7	MB1-DB5
14	PA-IO6	*TDO*	**VCCI**	PA-IO10	PA-IO14	PA-IO18	MA2-DB3	MA2-DB7	ADR0	ADR2	ADR4	WE	CSB	**VCCI**	MB1-DB3	MB1-DB1
15	*CCLK*	**GND**	**LED**	PA-IO13	PA-IO17	MA2-DB2	MA2-DB6	MA2-WRT	MA2-INT	DB1	DB3	DB5	DB7	OE/RST	**GND**	CE
16	**GND**	D0	PA-IO8	PA-IO11	PA-IO15	MA2-DB0	MA2-DB4	MA2-ASTB	MA2-WAIT	DB0	DB2	DB4	DB6	LDB CLK	CF	**GND**