

# Active Power Meter Reference Project



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## Overview

The Active Power Meter Reference Project provides a simple example of using the Multiply-Accumulate feature of Xilinx FPGA circuits. The module implements a power meter. Two input signals are sampled, representing a current and a voltage. Instant Power is computed as signed product of I and U samples. Active Power is then obtained by digital mediation (accumulated and divided by number of samples) of Instant Power samples, over the measurement period.

Instant and Active Powers are sent to DA converters for analysis. The Active Power is also shown on the seven segment display.

## Used Hardware and Digilent Library Reference Components

### Hardware Needed

- any Digilent FPGA system board with 6 or 12 pin connectors.
- one Pmod AD1
- one Pmod DA1
- one circuit to study, where U and I can be measured, using transducers. Even if the project works with DC and resistive loads also, AC and reactive loads (providing phase difference between current and voltage) make the experiment more spectacular. The measurement is accurate for any signal shape, not just sinusoidal waves, with either, or both, DC and AC components.
- an oscilloscope (and a voltmeter)
- external circuitry as described below

### Digilent Library Reference VHDL Components

- AD1 (for details, see the AD1 Reference Component)
- DA1 (for details, see the DA1 Reference Component)
- BinToBcdEncoder

### External Circuitry Required

... to convert the current I to a voltage signal VI in range 0 to 3.3V as follows:

- when  $I = 0\text{mA}$   $\Rightarrow V_I = 1.65\text{V}$
- when  $I = \text{MaxIValue}$  (positive)  $\Rightarrow V_I = 3.3\text{V}$
- when  $I = -\text{MaxIValue}$  (negative)  $\Rightarrow V_I = 0\text{V}$

... to scale the input voltage U to a voltage VU in range: 0 to 3.3V as follows:

- when  $U = 0\text{mV}$   $\Rightarrow VU = 1.65\text{V}$
- when  $U = \text{MaxUValue}$  (positive)  $\Rightarrow VU = 3.3\text{V}$
- when  $U = -\text{MaxUValue}$  (negative)  $\Rightarrow VU = 0\text{V}$

... to connect VI and VU to the voltage inputs of Pmod AD1.

...to connect the Pmod AD1 to the used Diligent system board.

## Behavioral Description

### Power Meter

This module is the top level of the project.

It instantiates an AD1 component for acquiring unsigned samples of:

- vecIUnsigned - digital image of VI
- vecUUnsigned - digital image of VU

The input vectors above are converted to signed vectors:

- vecISigned - digital image of I, normalized to range  $(-\text{MaxIValue}; +\text{MaxIValue})$
- vecUSigned - digital image of U, normalized to range  $(-\text{MaxUValue}; +\text{MaxUValue})$

The signed values above are supplied to MullAcc component, which returns:

- vecPinstSigned - digital image of the instant power Pinst, normalized to range  $(-\text{MaxPValue}; +\text{MaxPValue})$
- vecPSigned - digital image of the mean effective power over measurement period P, normalized to range  $(-\text{MaxPValue}; +\text{MaxPValue})$

In the ranges above,  $\text{MaxPValue} = \text{MaxIValue} * \text{MaxUValue}$ .

vecPinstSigned is converted to an unsigned value vecPinstUnsigned, which is sent to a DA1 Reference Component, which sends it further to a Pmod DA1.

The Pmod AD1 output signal VP, represents the instant power, shifted by 1.65V:

- when  $P_{\text{inst}} = 0$   $\Rightarrow VP = 1.65\text{V}$
- when  $P_{\text{inst}} = -\text{MaxPValue}$   $\Rightarrow VP = 0\text{V}$
- when  $P_{\text{inst}} = \text{MaxPValue}$   $\Rightarrow VP = 3.3\text{V}$

vecPSigned is converted to a "Sign and Magnitude" representation:

- bitPsign - the sign (0 for +, 1 for -)
- vecPMagnitude - the P absolute value

vecPMagnitude is scaled to vecPMagnitudeS with a range of  $(-1000; +1000)$ .

A BinToBcdEncoder\_nDigits Diligent Library Reference Component is instantiated to convert vecPMagnitudeS to the BCD representation vecPMagnitudeBcd, which is shown on the seven segment display.

The `vecPMagnitudeBcd`, represents the active power, scaled to  $\pm 1000$  :

- when `Pactive = 0`  $\Rightarrow$  `vecPMagnitudeBcd = 0`
- when `Pactive = -MaxPValue`  $\Rightarrow$  `vecPMagnitudeBcd = -999`
- when `Pactive = MaxPValue`  $\Rightarrow$  `vecPMagnitudeBcd = 999`

### **AD1RefComp, DA1RefComp, BinToBcdEncoder\_nDigits**

These are Diligent Library Reference Components. For more details about the behavior and usage of these components, see the AD1 Reference Component, DA1 Reference Component, and the source file comments.

For DA1 and DA1 Reference Components, no handshake is used. Instead, the start signal is long enough for both '1' and '0' level periods, to cover those components' timing requirements.

### **MulAcc**

Multiply accumulate component. It gets simultaneous samples of two analog signals:

- `vecI` = input current
- `vecU` = input voltage

Each couple of `vecI` and `vecU` is multiplied to get `vecPinst` = instant power.

$2^k$  `vecInstP` samples are added to get `vecE` = the active energy over the measurement period.

`vecE` is divided by the number of samples to get `vecP` = the active power.

Choosing a power of 2 as number of samples transforms the above division into shifting.

All `vecI`, `vecU`, `vecE`, `vecPinst`, and `vecP` are signed values.