

## Introduction

The Xilinx<sup>®</sup> XPS Universal Asynchronous Receiver Transmitter (UART) Lite Interface connects to the PLB (Processor Local Bus) and provides the controller interface for asynchronous serial data transfer. This soft IP core is designed to interface with the PLBV46.

## Features

- PLB interface is based on PLB v4.6 specification
- Supports 8-bit bus interfaces
- One transmit and one receive channel (full duplex)
- 16-character Transmit FIFO and 16-character Receive FIFO
- Configurable number of data bits in a character (5-8)
- Configurable parity bit (odd or even)
- Configurable baud rate

LogiCORE IP Facts Table				
Core Specifics				
Supported Device Family <sup>(1)</sup>	Virtex-5, Virtex-4, Spartan-3E, Automotive Spartan-3E, Spartan-3, Automotive Spartan-3, Spartan-3A, Spartan-3AN, Automotive Spartan-3A, Spartan-3A DSP, Automotive Spartan-3A DSP			
Supported User Interfaces	PLB v46			
Resources				
	Slices	LUTs	FFS	Block RAMs
See <a href="#">Table 9</a> , <a href="#">Table 10</a> and <a href="#">Table 11</a>				
Provided with Core				
Documentation	Product Specification			
Design Files	VHDL			
Example Design	Not Provided			
Test Bench	Not Provided			
Constraints File	N/A			
Simulation Model	N/A			
Tested Design Tools				
Design Entry Tools	ISE 13.2 software			
Simulation	Mentor Graphics ModelSim <sup>(2)</sup>			
Synthesis Tools	XST 13.2			
Support				
Provided by Xilinx @ <a href="http://www.xilinx.com/support">www.xilinx.com/support</a>				

1. For a complete listing of supported devices, see [IDS Embedded Edition Derivative Device Support](#) for this core.
2. For the supported versions of the tool, see the [ISE Design Suite 13: Release Notes Guide](#).

## Functional Description

The XPS UART Lite performs parallel-to-serial conversion on characters received through PLB and serial-to-parallel conversion on characters received from a serial peripheral.

The XPS UART Lite is capable of transmitting and receiving 8, 7, 6 or 5-bit characters, with 1-stop bit and odd, even or no parity. The XPS UART Lite can transmit and receive independently.

The device can be configured and its status can be monitored via the internal register set. The XPS UART Lite generates an interrupt when Receive FIFO becomes non-empty or when transmit FIFO becomes empty. This interrupt can be masked by using an interrupt enable/disable signal.

The device contains a 16-bit programmable baud rate generator and independent 16-word Transmit and Receive FIFOs. The FIFOs can be enabled or disabled through software control.

The XPS UART Lite modules are shown in the top-level block diagram in [Figure 1](#).

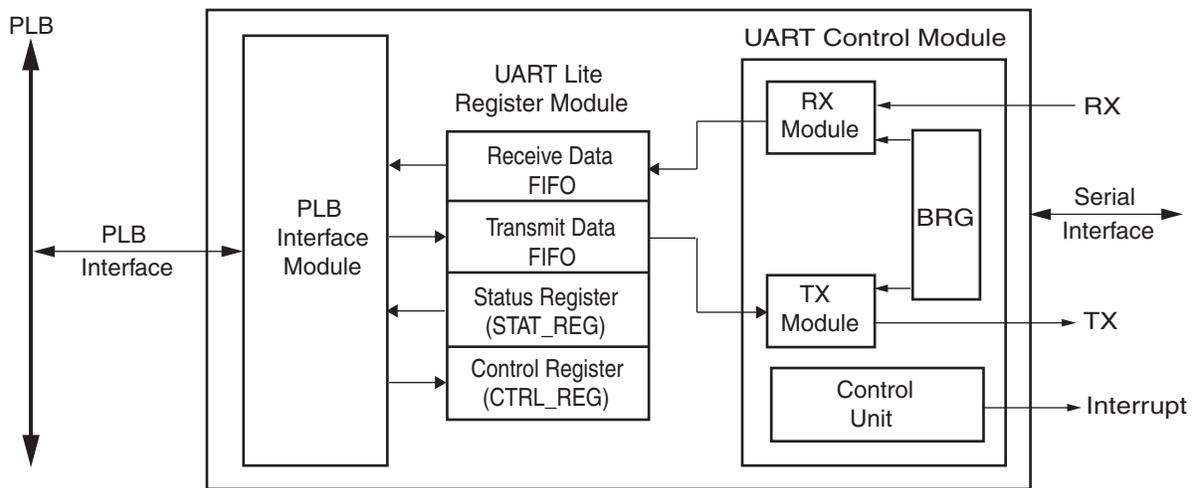


Figure 1: Block Diagram of XPS UART Lite

The XPS UART Lite modules are described in the next sections:

**PLB Interface Module:** The PLB Interface Module provides the interface to the PLB and implements PLB protocol logic. PLB Interface Module is a bidirectional interface between a user IP core and the PLB bus standard. To simplify the process of attaching an XPS UART Lite to the PLB, the core makes use of a portable, pre-designed bus interface called PLB Interface Module that takes care of the bus interface signals, bus protocols, and other interfaces.

**UART Lite Register Module:** The Register Module includes all memory-mapped registers (as shown in [Figure 1](#)). It interfaces to the PLB through the PLB Interface Module. It consists of an 8-bit status register, an 8-bit control register and a pair of 8-bit Transmit/Receive FIFOs. All registers are accessed directly from the PLB using the PLB Interface Module.

**UART Control Module:** The UART Control Module consists of an RX module, a TX module, a parameterized baud rate generator (BRG), and a Control Unit. It incorporates the state machine for initialization and start and stop bit control logic.

## Interrupts

If interrupts are enabled, an interrupt is generated when one of these two conditions is true:

1. When the Receive FIFO goes from empty to not empty, such as when the first valid character is received in the Receive FIFO
2. When the Transmit FIFO goes from not empty to empty, such as when the last character in the Transmit FIFO is transmitted

## XPS UART Lite I/O Signals

The XPS UART Lite I/O signals are listed and described in [Table 1](#).

**Table 1: XPS UART Lite I/O Signal Description**

Port	Signal Name	Interface	I/O	Initial State	Description
System Signals					
P1	SPLB_Clk	System	I	-	PLB clock
P2	SPLB_Rst	System	I	-	PLB reset, active high
PLB Interface Signals					
P3	PLB_ABus[0 : 31]	PLB	I	-	PLB address bus
P4	PLB_PAVValid	PLB	I	-	PLB primary address valid
P5	PLB_masterID[0 : C_SPLB_MID_WIDTH - 1]	PLB	I	-	PLB current master identifier
P6	PLB_RNW	PLB	I	-	PLB read not write
P7	PLB_BE[0 : (C_SPLB_DWIDTH/8) - 1]	PLB	I	-	PLB byte enables
P8	PLB_size[0 : 3]	PLB	I	-	PLB size of requested transfer
P9	PLB_type[0 : 2]	PLB	I	-	PLB transfer type
P10	PLB_wrDBus[0 : C_SPLB_DWIDTH - 1]	PLB	I	-	PLB write data bus
Unused PLB Interface Signals					
P11	PLB_UABus[0 : 31]	PLB	I	-	PLB upper address bits
P12	PLB_SAVValid	PLB	I	-	PLB secondary address valid
P13	PLB_rdPrim	PLB	I	-	PLB secondary to primary read request indicator
P14	PLB_wrPrim	PLB	I	-	PLB secondary to primary write request indicator
P15	PLB_abort	PLB	I	-	PLB abort bus request
P16	PLB_busLock	PLB	I	-	PLB bus lock
P17	PLB_MSize[0 : 1]	PLB	I	-	PLB data bus width indicator
P18	PLB_lockErr	PLB	I	-	PLB lock error
P19	PLB_wrBurst	PLB	I	-	PLB burst write transfer
P20	PLB_rdBurst	PLB	I	-	PLB burst read transfer

**Table 1: XPS UART Lite I/O Signal Description (Cont'd)**

Port	Signal Name	Interface	I/O	Initial State	Description
P21	PLB_wrPendReq	PLB	I	-	PLB pending bus write request
P22	PLB_rdPendReq	PLB	I	-	PLB pending bus read request
P23	PLB_wrPendPri[0 : 1]	PLB	I	-	PLB pending write request priority
P24	PLB_rdPendPri[0 : 1]	PLB	I	-	PLB pending read request priority
P25	PLB_reqPri[0 : 1]	PLB	I	-	PLB current request priority
P26	PLB_TAttribute[0 : 15]	PLB	I	-	PLB transfer attribute
PLB Slave Interface Signals					
P27	SI_addrAck	PLB	O	0	Slave address acknowledge
P28	SI_SSize[0 : 1]	PLB	O	0	Slave data bus size
P29	SI_wait	PLB	O	0	Slave wait
P30	SI_rearbitrate	PLB	O	0	Slave bus rearbitrate
P31	SI_wrDAck	PLB	O	0	Slave write data acknowledge
P32	SI_wrComp	PLB	O	0	Slave write transfer complete
P33	SI_rdBUS[0 : C_SPLB_DWIDTH - 1]	PLB	O	0	Slave read data bus
P34	SI_rdDAck	PLB	O	0	Slave read data acknowledge
P35	SI_rdComp	PLB	O	0	Slave read transfer complete
P36	SI_MBusy[0 : C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Slave busy
P37	SI_MWrErr[0 : C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Slave write error
P38	SI_MRdErr[0 : C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Slave read error
Unused PLB Slave Interface Signals					
P39	SI_wrBTerm	PLB	O	0	Slave terminate write burst transfer
P40	SI_rdWdAddr[0 : 3]	PLB	O	0	Slave read word address
P41	SI_rdBTerm	PLB	O	0	Slave terminate read burst transfer
P42	SI_MIRQ[0 : C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Master interrupt request
UART Lite Interface Signals					
P43	RX	UART Lite	I	-	Receive Data
P44	TX	UART Lite	O	0	Transmit Data
P45	Interrupt	UART Lite	O	0	UART Interrupt

## XPS UART Lite Design Parameters

To allow the user to obtain an XPS UART Lite that is uniquely tailored for the system, certain features can be parameterized in the XPS UART Lite design. This allows the user to configure a design that utilizes the resources required by the system only and that operates with the best possible performance. The features that can be parameterized in the XPS UART Lite design are as shown in [Table 2](#).

**Table 2: XPS UART Lite Design Parameters**

Generic	Feature/Description	Parameter Name	Allowable Values	Default Value	VHDL Type
System Parameter					
G1	Target FPGA family	C_FAMILY	spartan3e, aspartan3e, spartan3, aspartan3, spartan3a, spartan3an, aspartan3a, spartan3adsp, aspartan3adsp, virtex4, qvirtex4, qrvirtex4, virtex5	virtex5	string
G2	System clock frequency (in Hz) driving the UART Lite peripheral	C_SPLB_CLK_FREQ_HZ	integer (ex. 100000000)	100_000_000	Integer
PLB Parameters					
G3	PLB Base Address	C_BASEADDR	Valid Address <sup>(1)</sup>	None <sup>(3)</sup>	std_logic_vector
G4	PLB High Address	C_HIGHADDR	Valid Address <sup>(2)</sup>	None <sup>(3)</sup>	std_logic_vector
G5	PLB least significant address bus width	C_SPLB_AWIDTH	32	32	integer
G6	PLB data width	C_SPLB_DWIDTH	32, 64, 128	32	integer
G7	Selects point-to-point or shared bus topology	C_SPLB_P2P	0 = Shared Bus Topology 1 = Point-to-Point Bus Topology <sup>(4)</sup>	0	integer
G8	PLB Master ID Bus Width	C_SPLB_MID_WIDTH	$\log_2(\text{C\_SPLB\_NUM\_MASTERS})$ with a minimum value of 1	1	integer
G9	Number of PLB Masters	C_SPLB_NUM_MASTERS	1 - 16	1	integer
G10	Support Bursts	C_SPLB_SUPPORT_BURSTS	0	0	integer
G11	Width of the Slave Data Bus	C_SPLB_NATIVE_DWIDTH	32	32	integer
UART Lite Parameters					
G12	Baud rate of the UART Lite in bits per second	C_BAUDRATE	integer (ex. 128000)	128_000 <sup>&lt;RD Red&gt;[5]</sup>	Integer
G13	The number of data bits in the serial frame	C_DATA_BITS	5 - 8	8	Integer

Table 2: XPS UART Lite Design Parameters (Cont'd)

Generic	Feature/Description	Parameter Name	Allowable Values	Default Value	VHDL Type
G14	Determines whether parity is used or not	C_USE_PARITY	0 = Do not use parity 1 = Use parity	1	Integer
G15	If parity is used, determines whether parity is odd or even	C_ODD_PARITY	0 = Even parity 1 = Odd parity	1	Integer

**Notes:**

- The user must set the values. The C\_BASEADDR must be a multiple of the range, where the range is C\_HIGHADDR - C\_BASEADDR + 1.
- C\_HIGHADDR - C\_BASEADDR must be a power of 2 greater than equal to C\_BASEADDR + 0xF.
- No default value is specified to ensure that the actual value is set; that is, if the value is not set, a compiler error is generated.
- Value of '1' is not supported in this core.
- With a baud rate of 115200, the sample clock is  $16 * 115200 = 1.8432$  MHz. With the System clock C\_CLK\_FREQ running at 10 MHz, the integer ratio for driving the sample clock is 5 (rounding of  $[10/1.8432]$ ). The UART Lite then divides the System clock by 5 resulting in 2 MHz for the sample clock. The baud rate error is  $(1.8432 - 2) / 1.8432 \Rightarrow -8.5\%$  which is outside the tolerance for most UARTs. The issue is that the higher the baud rate and the lower the C\_CLK\_FREQ, the greater the error in the generated baud rate of the UART Lite. Specifications for the baud rate error state that within 5% of the requested rate is considered acceptable.

**Allowable Parameter Combinations**

The address range specified by C\_BASEADDR and C\_HIGHADDR must be a power of 2, and must be at least 0xF.

For example, if C\_BASEADDR = 0xE0000000, C\_HIGHADDR must be at least = 0xE000000F.

**XPS UART Lite Parameter - Port Dependencies**

The dependencies between the XPS UART Lite core design parameters and I/O signals are described in Table 3. In addition, when certain features are parameterized out of the design, the related logic will no longer be a part of the design. The unused input signals and related output signals are set to a specified value.

Table 3: XPS UART Lite Parameter-Port Dependencies

Generic or Port	Name	Affects	Depends	Relationship Description
Design Parameters				
G6	C_SPLB_DWIDTH	P7, P10, P33	-	Affects the number of bits in data bus
G8	C_SPLB_MID_WIDTH	P5	G9	This value is calculated as: $\log_2(\text{C\_SPLB\_NUM\_MASTERS})$ with a minimum value of 1
G9	C_SPLB_NUM_MASTERS	P36, P37, P38, P42	-	Affects the number of PLB masters
I/O Signals				
P5	PLB_masterID[0 : C_SPLB_MID_WIDTH - 1]	-	G8	Width of the PLB_mastedID varies according to C_SPLB_MID_WIDTH
P7	PLB_BE[0 : (C_SPLB_DWIDTH/8) - 1]	-	G6	Width of the PLB_BE varies according to C_SPLB_DWIDTH
P10	PLB_wrDBus[0 : C_SPLB_DWIDTH - 1]	-	G6	Width of the PLB_wrDBus varies according to C_SPLB_DWIDTH
P33	SI_rdDBus[0 : C_SPLB_DWIDTH - 1]	-	G6	Width of the SI_rdDBus varies according to C_SPLB_DWIDTH

Table 3: XPS UART Lite Parameter-Port Dependencies (Cont'd)

Generic or Port	Name	Affects	Depends	Relationship Description
P36	SI_MBusy[0 : C_SPLB_NUM_MASTERS - 1]	-	G9	Width of the SI_MBusy varies according to C_SPLB_NUM_MASTERS
P37	SI_MWrErr[0 : C_SPLB_NUM_MASTERS - 1]	-	G9	Width of the SI_MWrErr varies according to C_SPLB_NUM_MASTERS
P38	SI_MRdErr[0 : C_SPLB_NUM_MASTERS - 1]	-	G9	Width of the SI_MRdErr varies according to C_SPLB_NUM_MASTERS
P42	SI_MIRQ[0 : C_SPLB_NUM_MASTERS - 1]	-	G9	Width of the SI_MIRQ varies according to C_SPLB_NUM_MASTERS

## XPS UART Lite Register Descriptions

Table 4 shows all the XPS UART Lite registers and their addresses.

Table 4: XPS UART Lite Registers

Base Address + Offset (hex)	Register Name	Access Type	Default Value (hex)	Description
C_BASEADDR + 0x0	Rx FIFO <sup>(3)</sup>	Read <sup>(1)</sup>	0x0	Receive Data FIFO
C_BASEADDR + 0x4	Tx FIFO <sup>(3)</sup>	Write <sup>(2)</sup>	0x0	Transmit Data FIFO
C_BASEADDR + 0x8	STAT_REG <sup>(3)</sup>	Read <sup>(1)</sup>	0x4	UART Lite Status Register
C_BASEADDR + 0xC	CTRL_REG <sup>(3)</sup>	Write <sup>(2)</sup>	0x0	UART Lite Control Register

1. Writing of a read only register has no effect.
2. Reading of a write only register returns zero.
3. Registers are defined for full 32-bit access only. Any partial word accesses (byte or halfword) have undefined results and returns a bus error.

## Receive Data FIFO

This 16 entry deep FIFO contains data to be received by XPS UART Lite. The FIFO bit definitions are shown in Table 5. Reading of this location will result in reading the current word out from the FIFO. When a read request is issued to an empty FIFO a bus error is generated and the result is undefined. The Receive Data FIFO is a read-only register. Issuing a write request to Receive Data FIFO will do nothing but generate the write acknowledgement. Figure 2 shows the location for data on the PLB when C\_DATA\_BITS is set to 8.



Figure 2: Receive Data FIFO (C\_DATA\_BITS = 8)

Table 5: Receive Data FIFO Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
0 - [31-C_DATA_BITS]	Reserved	N/A	0	Reserved
[(31-C_DATA_BITS)+1] - 31	Rx Data	Read	0	UART Receive data

### Transmit Data FIFO

This 16 entry deep FIFO contains data to be output by XPS UART Lite. The FIFO bit definitions are shown in Table 6. Data to be transmitted is written into this register. This is write only location. Issuing a read request to Transmit Data FIFO generates the read acknowledgement with zero data. Figure 3 shows the location for data on the PLB when C\_DATA\_BITS is set to 8.

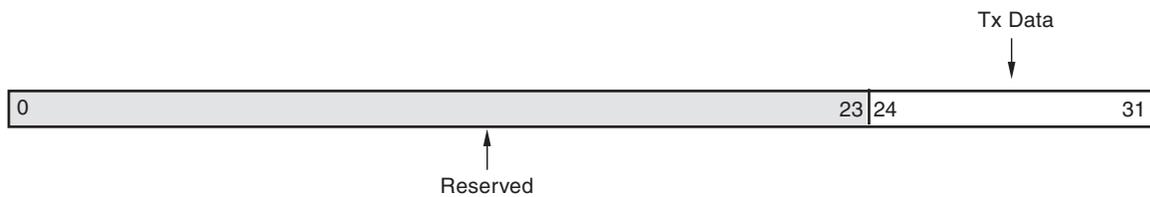


Figure 3: Transmit Data FIFO (C\_DATA\_BITS = 8)

Table 6: Transmit Data FIFO Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
0 - [31-C_DATA_BITS]	Reserved	N/A	0	Reserved
[(31-C_DATA_BITS)+1] - 31	Tx Data	Write	0	UART transmit data

### UART Lite Control Register (CTRL\_REG)

The UART Lite Control Register contains the Enable Interrupt bit and Reset pin for Receive and Transmit Data FIFO. This is write only register. Issuing a read request to Control Register generates the read acknowledgement with zero data. Figure 4 shows the bit assignment of the CTRL\_REG. Table 7 describes this bit assignment.



Figure 4: UART Lite Control Register

Table 7: UART Lite Control Register Bit Definitions

Bit(s)	Name	Core Access	Reset Value	Description
0 - 26	Reserved	N/A	0	Reserved
27	Enable Intr	Write	'0'	Enable Interrupt for the UART Lite '0' = Disable interrupt signal '1' = Enable interrupt signal
28 - 29	Reserved	N/A	0	Reserved
30	Rst Rx FIFO	Write	'0'	Reset/Clear the Receive FIFO Writing a '1' to this bit position clears the Receive FIFO '0' = Do nothing '1' = Clear the Receive FIFO
31	Rst Tx FIFO	Write	'0'	Reset/Clear the Transmit FIFO Writing a '1' to this bit position clears the Transmit FIFO '0' = Do nothing '1' = Clear the Transmit FIFO

### UART Lite Status Register (STAT\_REG)

The UART Lite Status Register contains the status of the Receive and Transmit Data FIFO, if interrupts are enabled, and if there are any errors. This is read only register. If a write request is issued to status register it will do nothing but generate write acknowledgement. Bit assignment in the STAT\_REG is shown in Figure 5 and described in Table 8.

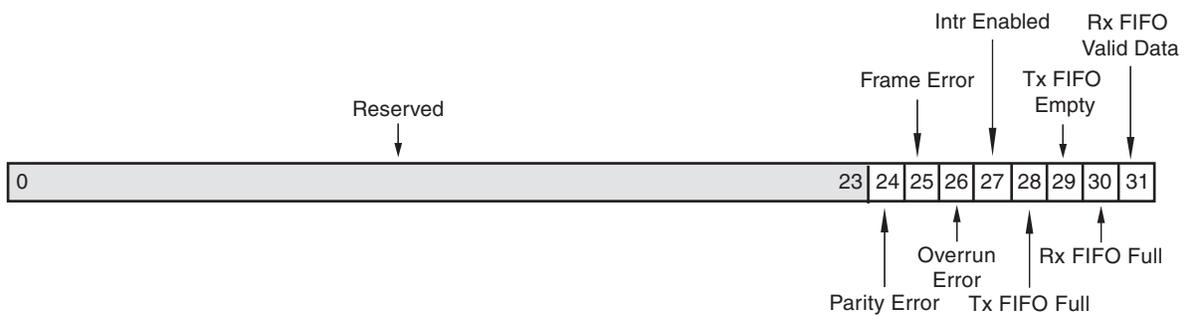


Figure 5: UART Lite Status Register

**Table 8: UART Lite Status Register Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
0 - 23	Reserved	N/A	0	Reserved
24	Parity Error	Read	'0'	Indicates that a parity error has occurred after the last time the status register was read. If the UART is configured without any parity handling, this bit is always '0'. The received character is written into the Receive FIFO. This bit is cleared when the status register is read '0' = No parity error has occurred '1' = A parity error has occurred
25	Frame Error	Read	'0'	Indicates that a frame error has occurred after the last time the status register was read. Frame Error is defined as detection of a stop bit with the value '0'. The receive character is ignored and not written to the Receive FIFO. This bit is cleared when the status register is read '0' = No Frame error has occurred '1' = A frame error has occurred
26	Overrun Error	Read	'0'	Indicates that a overrun error has occurred since the last time the status register was read. Overrun is when a new character has been received but the Receive FIFO is full. The received character is ignored and not written into the Receive FIFO. This bit is cleared when the status register is read '0' = No interrupt has occurred '1' = Interrupt has occurred
27	Intr Enabled	Read	'0'	Indicates that interrupts is enabled '0' = Interrupt is disabled '1' = Interrupt is enabled
28	Tx FIFO Full	Read	'0'	Indicates if the Transmit FIFO is full '0' = Transmit FIFO is not full '1' = Transmit FIFO is full
29	Tx FIFO Empty	Read	'1'	Indicates if the Transmit FIFO is empty '0' = Transmit FIFO is not empty '1' = Transmit FIFO is empty
30	Rx FIFO Full	Read	'0'	Indicates if the Receive FIFO is full '0' = Receive FIFO is not full '1' = Receive FIFO is full
31	Rx FIFO Valid Data	Read	'0'	Indicates if the receive FIFO has valid data '0' = Receive FIFO is empty '1' = Receive FIFO has valid data

## Design Implementation

### Target Technology

The intended target technology is Virtex®-4, Virtex-5 and Spartan®-3 family FPGAs.

### Device Utilization and Performance Benchmarks

#### Core Performance

Because the XPS UART Lite core will be used with other design modules in the FPGA, the utilization and timing numbers reported in this section are estimates only. When the XPS UART Lite core is combined with other designs in the system, the utilization of FPGA resources and timing of the XPS UART Lite design will vary from the results reported here.

The XPS UART Lite resource utilization for various parameter combinations measured with Virtex-4 FPGAs as the target device are detailed in [Table 9](#).

**Table 9: Performance and Resource Utilization Benchmarks on Virtex-4 (xc4vlx25-10-ff668)**

Parameter Values (other parameters at default value)						Device Resources			Performance
C_SPLB_AWIDTH	C_CLK_FREQ	C_BAUDRATE	C_DATA_BITS	C_USE_PARITY	C_ODD_PARITY	Slices	Slice Flip-Flops	LUTs	F <sub>MAX</sub> (MHz)
32	100_000_000	19_200	5	FALSE	FALSE	98	83	123	145
32	100_000_000	19_200	6	FALSE	FALSE	100	84	127	132
32	100_000_000	19_200	7	FALSE	FALSE	100	85	129	168
32	100_000_000	19_200	8	FALSE	FALSE	101	86	131	122
32	40_000_000	38_400	8	FALSE	FALSE	100	85	130	125
32	100_000_000	19_200	6	TRUE	FALSE	104	90	134	117
32	100_000_000	19_200	7	TRUE	FALSE	105	91	136	149

The XPS UART Lite resource utilization for various parameter combinations measured with Virtex-5 FPGAs as the target device are detailed in [Table 10](#).

**Table 10: Performance and Resource Utilization Benchmarks on Virtex-5 (xc5vlx85-1-ff1153)**

Parameter Values (other parameters at default value)						Device Resources			Performance
C_SPLB_AWIDTH	C_CLK_FREQ	C_BAUDRATE	C_DATA_BITS	C_USE_PARITY	C_ODD_PARITY	Slices	Slice Flip-Flops	LUTs	f <sub>MAX</sub> (MHz)
32	100_000_000	19_200	5	FALSE	FALSE	97	90	137	126
32	100_000_000	19_200	6	FALSE	FALSE	92	85	137	119
32	100_000_000	19_200	7	FALSE	FALSE	91	85	130	158
32	100_000_000	19_200	8	FALSE	FALSE	96	86	139	115
32	40_000_000	38_400	8	FALSE	FALSE	92	85	137	119
32	100_000_000	19_200	6	TRUE	FALSE	97	90	137	126
32	100_000_000	19_200	7	TRUE	FALSE	99	91	139	116

The XPS UART Lite resource utilization for various parameter combinations measured with Spartan-3E FPGAs as the target device are detailed in [Table 11](#).

**Table 11: Performance and Resource Utilization Benchmarks on Spartan-3E (xc3s250e-4-ft256)**

Parameter Values (other parameters at default value)						Device Resources			Performance
C_SPLB_AWIDTH	C_CLK_FREQ	C_BAUDRATE	C_DATA_BITS	C_USE_PARITY	C_ODD_PARITY	Slices	Slice Flip-Flops	LUTs	f <sub>MAX</sub> (MHz)
32	100_000_000	19_200	5	FALSE	FALSE	97	83	125	108
32	100_000_000	19_200	6	FALSE	FALSE	98	84	129	102
32	100_000_000	19_200	7	FALSE	FALSE	97	83	125	108
32	100_000_000	19_200	8	FALSE	FALSE	98	84	129	102
32	40_000_000	38_400	8	FALSE	FALSE	100	85	131	117
32	100_000_000	19_200	6	TRUE	FALSE	106	90	136	108
32	100_000_000	19_200	7	TRUE	FALSE	100	85	131	117

### System Performance

To measure the system performance (Fmax) of this core, this core was added to a Virtex-4 FPGA system, a Virtex-5 FPGA system, and a Spartan-3A FPGA system as the Device Under Test (DUT) as shown in [Figure 6](#), [Figure 7](#), and [Figure 8](#).

Because the XPS UART Lite core will be used with other design modules in the FPGA, the utilization and timing numbers reported in this section are estimates only. When this core is combined with other designs in the system, the utilization of FPGA resources and timing of the design will vary from the results reported here.

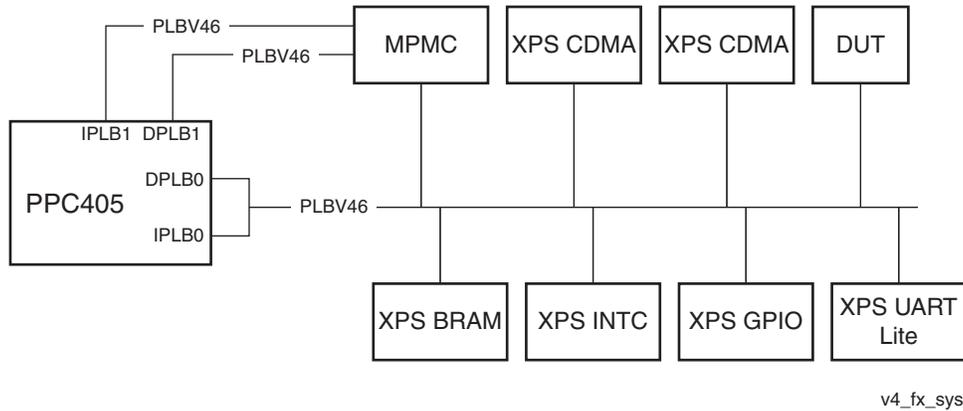


Figure 6: Virtex-4 FX System

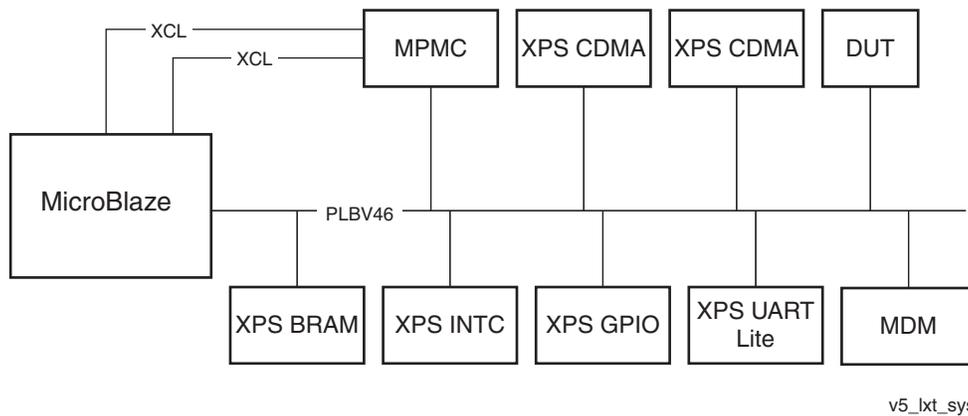


Figure 7: Virtex-5 LX System

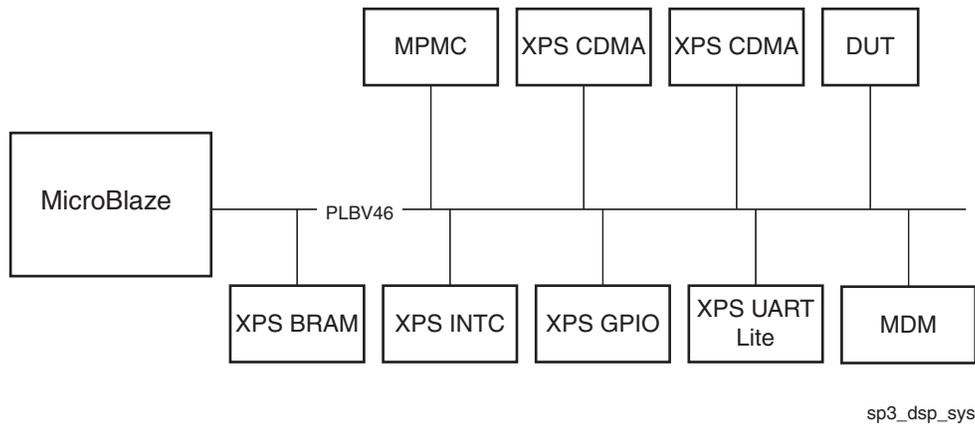


Figure 8: Spartan-3A System

The target FPGA was then filled with logic to drive the LUT and block RAM utilization to approximately 70% and the I/O utilization to approximately 80%. Using the default tool options and the slowest speed grade for the target FPGA, the resulting target Fmax numbers are shown in Table 12.

Table 12: XPS UART Lite System Performance

Target FPGA	Target $f_{MAX}$ (MHz)
S3A700 -4	90
V4FX60 -10	100
V5LXT50 -1	120

The target Fmax is influenced by the exact system and is provided for guidance. It is not a guaranteed value across all systems.

## Ordering Information

This Xilinx LogiCORE IP module is provided at no additional cost with the Xilinx ISE Design Suite Embedded Edition software under the terms of the [Xilinx End User License](#). The core is generated using the Xilinx ISE Embedded Edition software (EDK).

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## Reference Documents

IBM CoreConnect 128-Bit Processor Local Bus, Architectural Specification (v4.6).

## List of Acronyms

Acronym	Spelled Out
BRG	Baud Rate Generator
DSP	Digital Signal Processing
DUT	Device Under Test
FF	Flip-Flop
FIFO	First In First Out
FMAX	Maximum Frequency
FPGA	Field Programmable Gate Array
I/O	Input Output
LUT	Lookup Table
MHz	MegaHertz
PLB	Processor Local Bus
RAM	Random Access Memory
RX	Receive
TX	Transmit
UART	Universal Asynchronous Receiver Transmitter
XPS	Xilinx Platform Studio

## Revision History

Date	Version	Revision
4/18/07	1.0	Initial Xilinx release.
4/20/07	1.1	Added SP-3 support.
9/26/07	1.2	Added FMax Margin <RD Red>System Performance section.
11/27/07	1.3	Added SP3A DSP to supported devices listing.
1/14/08	1.4	Added Virtex-II Pro support.
4/21/08	1.5	Added Automotive Spartan-3E, Automotive Spartan-3A, Automotive Spartan-3, and Automotive Spartan-3A DSP support.
7/18/08	1.6	Added QPro Virtex-4 Hi-Rel and QPro Virtex-4 Rad Tolerant FPGA support.
9/20/08	1.7	Updated to version v1.01a. Removed Virtex-II Pro support. Modified Interrupts and Register description sections.
6/22/11	1.8	Updated to version v1.02a. Updated the interrupts section.

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