Anvyl Demonstration Projects

Revision: May 22, 2013
Note: This document applies to REV B of the board

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Overview

This package of demonstration projects can be used to illustrate all the features of the Anvyl FPGA development platform. Each chapter of this document will provide a brief overview for a basic demonstration of some of the Anvyl's components and capabilities. In each chapter, there are details of the hardware required, version of Xilinx tools required, included support files and instructions to perform the demonstrations.

The *Anvyl_Demo* zipped folder contains this manual and directories for each chapter. In each chapter directory there are source files, compiled bit files, and documentation files for any additional hardware used. All projects were developed in Xilinx ISE and EDK 13.4 but will migrate to 14.4 without complication.

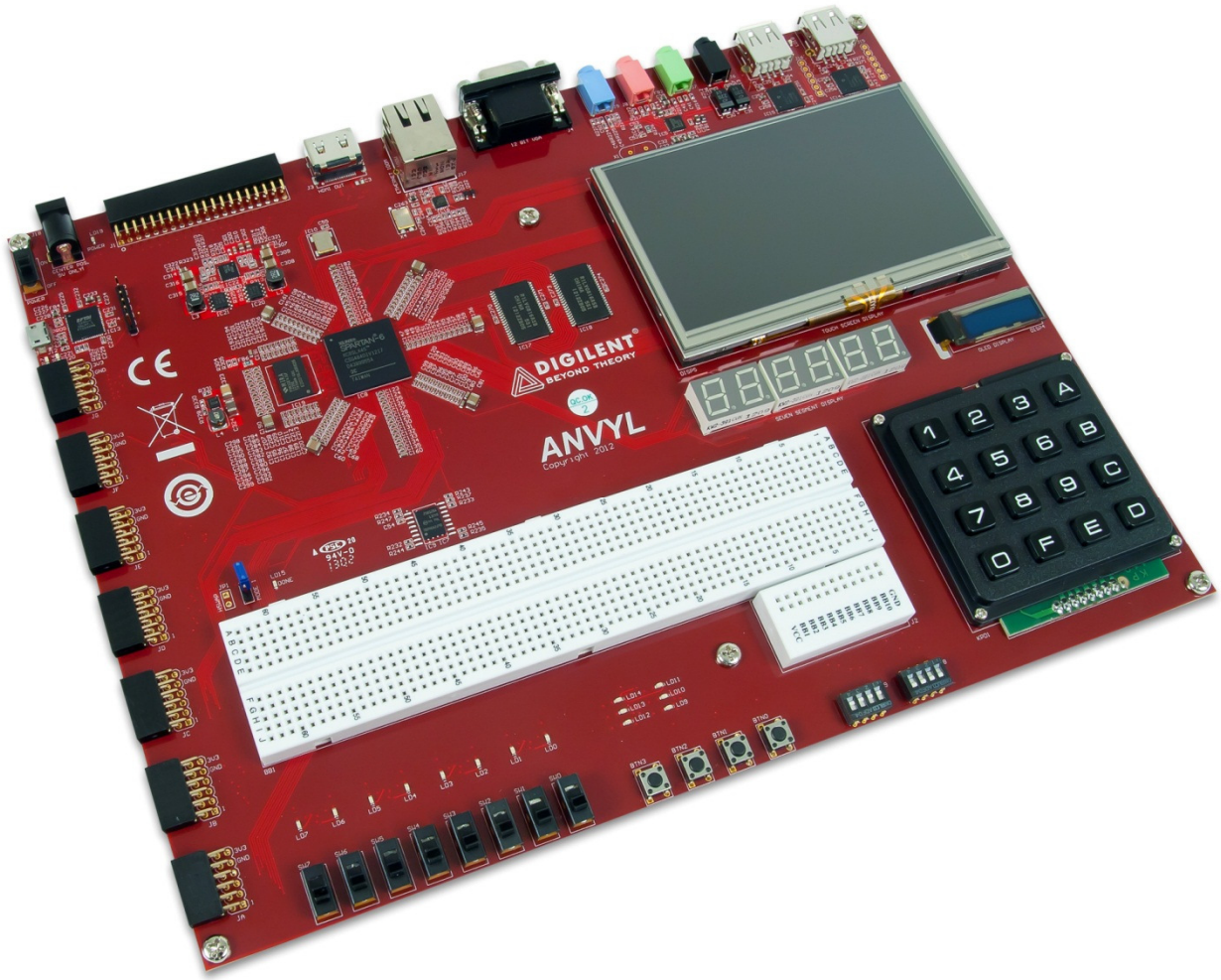

Fig. 1. *Anvyl FPGA development platform.*

Table of Contents

Setting up and programming the Anvyl

In every chapter, the board will need to be setup and programmed. This section describes how to accomplish this.

Hardware Required:

- Anvyl Development board
- USB A to micro B cable
- 5V 4A Power Supply

Software Required:

- Digilent Adept System for Windows

Instructions:

1. Connect the 5V 4A Power Supply to the Anvyl
2. Connect the USB A to USB Micro B cable to the USB port on the Anvyl (J12) below the power switch
3. Switch the power switch up or high on the Anvyl. The Power LED (LD19) will be illuminated
4. Move switch 0 (SW0) to the up or high position
5. Move all other switches(SW1-7) to the down or low position
6. Open Digilent Adept
   - Start -> All Programs -> Digilent -> Adept.

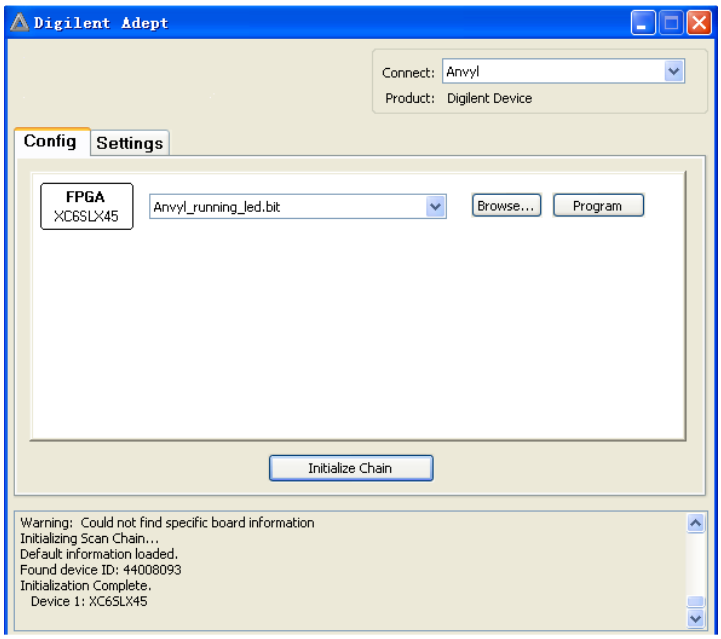

Fig. 2. *Adept programming software.*

7. Adept will try to initialize itself for device configuration automatically but it can also be initialized manually by clicking on the “initialize chain” button.

8. Select Anvyl from the drop down menu labeled “Connect’
   - If Adept does not recognize the board, unplug it, plug it back in and try again.
9. In the “Config” tab, click “Browse” and navigate to the folder containing the demo projects
10. Navigate to and open the bit file in the demo folder (example: “Anvyl_Demos” -> “01.Anvyl_SW_LED_Demo” -> “bitfile” -> “Anvyl_running_led.bit”)
11. click “Program” to program the Anvyl with the selected bit file
12. When the “DONE” LED (LD15) is lit, the Anvyl is programmed with the selected bit file and is ready for testing

Chapter 1: Running LED Demo

This is a simple demo that changes the status of the user LEDs (LD0-7).

Additional Hardware Required:
- none

Software Platforms:
- Xilinx ISE 13.4

Supplied Files:
- Programming bit file
- ISE project files

Instructions:
1. Setup and program the board as described in the “Setting up and programming the Anvyl” section

The LEDs 0-7 (LD0-7) will illuminate in ascending order till they are all on then they will turn off in ascending order. The speed of the LED cycle can be changed by flipping the user switches (SW0-2).

Chapter 2: Counter (stopwatch) Demo

This demo will utilize the seven segment display to produce a stop watch timer. This will allow the user to observe the functionality of the seven segment display and interact with it using the user buttons.

Additional Hardware Required:
- none

Software Platforms:
- Xilinx ISE 13.4

Supplied Files:
- Programming bit file
- ISE project files

Instructions:
1. Setup and program the board as described in the “Setting up and programming the Anvyl” section

The six digits of the seven segment display are used like a stopwatch and can be controlled using:
- Use SW0 to illuminate the seven segment displays
- BTN0 starts the counter
- BTN1 stops the counter
- BTN2 increments the counter when stopped
- toggling SW7 will reset the counter

The seven segment counter will act like a stopwatch and continue to count till it is stopped or reset. When the timer is stopped, it can be incremented by one millisecond and the timer can be resumed by pressing BTN0. Once the timer gets to “999999” then it is will start over at “0”. SW0 can be toggled to reset the clock.

Chapter 3: Keypad & Seven Segment Demo

This demo is shows off the seven segments display and allows the user to change the display by pushing buttons on the on board keypad on the Anvyl.

Additional Hardware Required:
- none

Software Platforms:
- Xilinx ISE 13.4

Supplied Files:
- Programming bit file
- ISE project files
- The project files contain several .coe files to initialize memory block including initial message“123456”

Instructions:
1. Setup and program the board as described in the “Setting up and programming the Anvyl” section

This demo displays the input from the keypad on the six seven segment LED displays. The display will initialize with “123456” and when the user presses a button. It will change the left most digit to the value of the pressed button. Each additional button press will change the digit to the right of the previous digit and wrap around once the last digit has been used.

Example:
SW0 is high and display initializes as “123456”
1. Button “9” is pressed and the seven segment display will be "923456”
2. Button "3" is pressed and the seven segment display will be "933456"
3. Button "F" is pressed and the seven segment display will be "93F456"

Chapter 4: OLED Demo

This demo shows off the capabilities of the 128 x 32 dot matrix OLED display on the Anvyl.

Additional Hardware Required:
- none

Software Platforms:
- Xilinx ISE 13.4

Supplied Files:
- Programming bit file
- ISE project files
- PmodOLED Interface Reference Project target on Nexys 3
- .coe file for initialization of the memory block
- dot matrix information of the logo and picture

Instructions
1. Setup and program the board as described in the “Setting up and programming the Anvyl” section

The OLED will switch through three different pictures displaying text or pictures. SW0 is a reset for the display and will turn off the display all other switches should be set to low.

Fig. 3. *Adept programming software.*

Note: sometimes the display will stay off although the SW0 set has been flipped from low to high. Flipping the switch will fix the issue.

Chapter 5: Memory Test Demo

This demo utilizes Xilinx EDK to produce a MicroBlaze project to test whether the SRAM and DDR are functioning correctly and outputs the results over UART to a hyper terminal client.

Additional Hardware Required:
- none

Software Platforms:
- Xilinx EDK 13.4
- Hyper terminal client

Supplied Files:
- Programming bit file
- Xilinx Platform Studio files
- EDK project file

Instructions:
1. Setup and program the board as described in the “Setting up and programming the Anvyl” section
2. Open a hyper terminal
    a. settings:
        - Baud rate: 115200
        - Data bit: 8 bit
        - Parity: none
        - Stop bit: 1 bit
        -

If memory is successfully programmed, it will display a message like this:

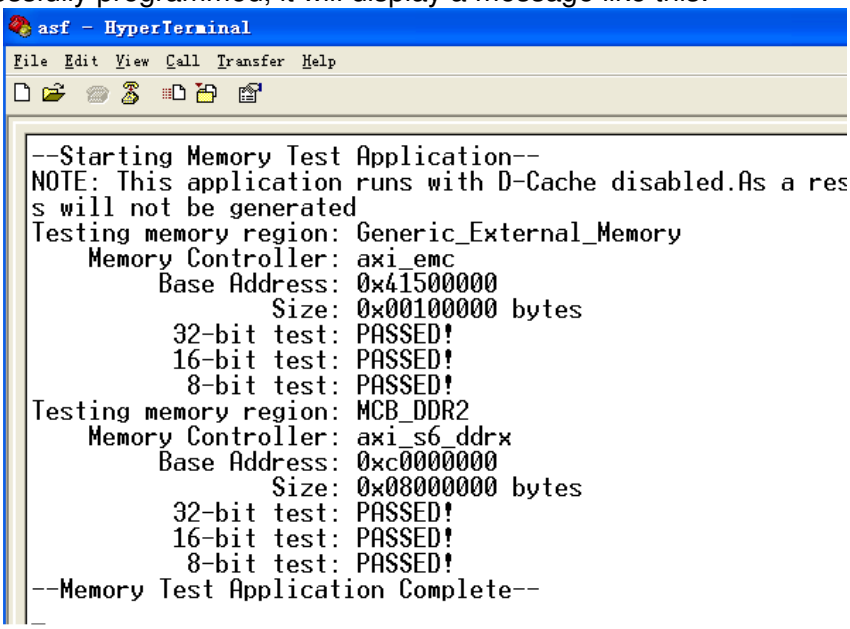

Fig. 4. *Successful memory test.*

Chapter 6: VGA Demo

This demo uses the VGA capabilities of the Anvyl to display green and blue stripes on a computer monitor (640 x 480 @ 60Hz).

Additional Hardware Required:
- VGA cable and monitor

Software Platforms:
- Xilinx ISE 13.4
- Hyper terminal client

Supplied Files:
- Programming bit file
- Xilinx Platform Studio files
- EDK project files

Instructions:
1. Connect the VGA cable to port J4 on the Anvyl and the other end to a VGA compatible monitor
2. Setup and program the board as described in the “Setting up and programming the Anvyl” section

The monitor will display a blue and green vertical line pattern on the screen.

Chapter 7: TFT Touch Panel Demo

This demo shows off the capabilities of the TFT touch screen panel on the Anvyl. The user will be able to use the touch screen to draw on the TFT panel.

Additional Hardware Required:
- none

Software Platforms:
- Xilinx ISE 13.4

Supplied Files:
- Programming bit file
- ISE project files

Instructions:
1. Switches 4-7(SW4-7) need to be initially set high
2. Switches 0-3(SW0-3) need to be initially set low
3. Setup and program the board as described in the “Setting up and programming the Anvyl” section. Ignore the switch configuration instructions.

The TFT touch screen will be interactive with the touch of a finger. Switches 4-6 (SW4 – SW6) control the intensity of the screen backlight. Switch 7(SW7) turns on and off the TFT backlight

Chapter 8: Audio Demo

This demo plays audio from the I2S audio codec on the Anvyl. Given an analog signal, the Anvyl will produce an unfiltered signal out of either the headphone port or line out port.

Additional Hardware Required:
- Audio cables
- Speaker or headphones

Software Platforms:
- Xilinx EDK 13.4

Supplied Files:
- Three different programming bit file
- ISE project files
- EDK project files
- Telnet client

Instructions:
1. Connect an audio source to the “LINE IN” port (J9) and a speaker or headphones to the headphone port.
2. Setup and program the board with the “bypass.bit” file as described in the “Setting up and programming the Anvyl” section
3. The speaker will produce the input audio signal from “HEADPHONE” port
4. Next change the speaker or headphones to the “LINE OUT” port and program the board with “0dbin_6dbout.bit”.
5. Audio will be produced from the “LINE OUT” port and will be softer than before.
6. Program the board with “33dbin_6dbout.bit” and the audio produced will be louder than the previous program.

Chapter 9: HDMI Demo

This is an EDK demo that uses the HDMI port to display a red and green background with a bouncing Digilent logo to an HDMI or DVI capable monitor.

Additional Hardware Required:
- HDMI cable or HDMI to DVI cable
- HDMI/DVI capable monitor

Software Platforms:
- Xilinx EDK 13.4

Supplied Files:
- Programming bit file
- ISE project files
- EDK project files

Instructions:
1. Connect the HDMI end of the cable to the Anvyl HDMI port (J3).
2. Connect the other end of the cable to the monitor
3. Setup and program the board as described in the “Setting up and programming the Anvyl” section

The monitor will display a green and red vertically striped background with a floating Digilent emblem.

Chapter 10: Ethernet Demo

This is an EDK project based on the MicroBlaze processor. It involves the axi_ethernetlite, mii_to_rmii, AXI_INTC and AXI_TIMER Xilinx pcores. In this demo, the user will host an echo server on the Anvyl board.

Additional Hardware Required:
- Ethernet cable (with RJ 45 connector)

Software Platform:
- Xilinx EDK 13.4

Supplied Files:
- Programming bit file
- ISE project files
- EDK project files

Instructions:
1. Plug an Ethernet cable from the computer to the Ethernet port on the Anvyl (J17)
2. Setup and program the board as described in the "Setting up and programming the Anvyl" section
3. Open a hyper terminal and select the corresponding COM port.
    a. Baud rate: 115200
    b. Parity: none
    c. Data bit: 8
    d. Flow control: none
    e. Stop: 1 bit
4. Navigate and run XMD as administrator. It is located at C:/Xilinx/14.4/ISE_DS/EDK/bin/nt/xmd.exe

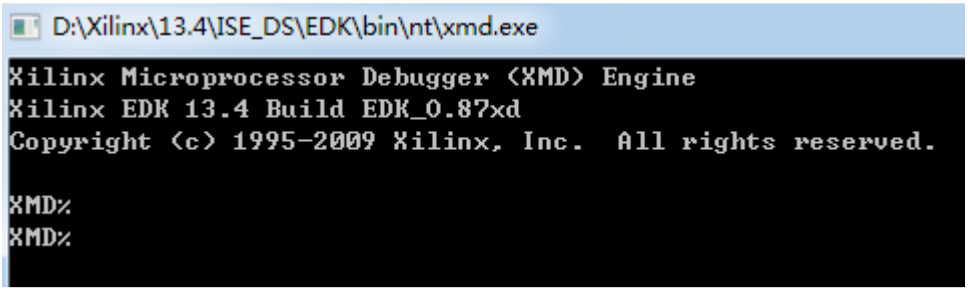

Fig. 5. *Xmd.exe.*

5. Connect to the MicroBlaze through JTAG
    a. "connect mb mdm"

```
XMD%
XMD% connect mb mdm

JTAG chain configuration
--------------------------------------------------
Device   ID Code         IR Length    Part Name
 1       44008093           6         XC6SLX45

MicroBlaze Processor Configuration :
-------------------------------------
Version.............................8.20.b
Optimization........................Performance
Interconnect........................PLB_v46
MMU Type............................No_MMU
No of PC Breakpoints................1
No of Read Addr/Data Watchpoints...0
No of Write Addr/Data Watchpoints..0
Instruction Cache Support..........off
Data Cache Support..................off
Exceptions  Support.................off
FPU  Support........................off
Hard Divider Support................off
Hard Multiplier Support............on - (Mul32)
Barrel Shifter Support..............on
MSR clr/set Instruction Support....on
Compare Instruction Support........on
Data Cache Write-back Support......off
Fault Tolerance Support............off
Stack Protection Support...........off

Connected to "mb" target. id = 0
Starting GDB server for "mb" target (id = 0) at TCP port no 1234
XMD%
```

Fig. 6. *Connect to MicroBlaze.*

6. Navigate to where the demo folder was placed
    a. Example for folder on desktop: “cd C:/Users/jsmith/Desktop/”Anvyl_Demos”/10.Anvyl_Ethernet_Demo/bitfile”

```
Connected to "mb" target. id = 0
Starting GDB server for "mb" target (id = 0) at TCP port no 1234
XMD% cd D:/hc_work/Anvyl/Anvyl_CD/02.Demos/10.Anvyl_Ethernet_Demo/bitfile
XMD% ls
download.bit  lwip_echo_server_0.elf
XMD%
```

Fig. 7.*Change the directory.*

7. Download the .elf file
    a. “dow lwip_echo.elf”

```
XMD% dow lwip_echo_server_0.elf
Downloading Program -- lwip_echo_server_0.elf
        section, .vectors.reset: 0x00000000-0x00000007
        section, .vectors.sw_exception: 0x00000008-0x0000000f
        section, .vectors.interrupt: 0x00000010-0x00000017
        section, .vectors.hw_exception: 0x00000020-0x00000027
        section, .text: 0x88000000-0x8801b707
        section, .init: 0x8801b708-0x8801b747
        section, .fini: 0x8801b748-0x8801b767
        section, .ctors: 0x8801b768-0x8801b76f
        section, .dtors: 0x8801b770-0x8801b777
        section, .rodata: 0x8801b778-0x8801c63b
        section, .sdata2: 0x8801c63c-0x8801c63f
        section, .data: 0x8801c640-0x8801cbe7
        section, .eh_frame: 0x8801cbe8-0x8801cbeb
        section, .jcr: 0x8801cbec-0x8801cbef
        section, .bss: 0x8801cbf0-0x880b3f5f
        section, .heap: 0x880b3f60-0x881b3f5f
        section, .stack: 0x881b3f60-0x882b3f5f
Setting PC with Program Start Address 0x00000000
System Reset .... DONE

XMD%
```

Fig. 8. *LWIP ECHO application downlaoded to the Anvyl.*

8. Run the package
    a. “run”

```
-----lwIP TCP echo server ------
TCP packets sent to port 6001 will be echoed back
Board IP: 192.168.1.10
Netmask : 255.255.255.0
Gateway : 192.168.1.1
auto-negotiated link speed: 100
TCP echo server started @ port 7
```

```
D:\Xilinx\14.2\ISE_DS\EDK\bin\nt\xmd.exe

XMD% run
Processor started. Type "stop" to stop processor

RUNNING> 0
```

Fig. 9. *Run LWIP echo and Hyper Terminal.*

The LWIP echo server has been successfully run on the Anvyl. In the hyper terminal, there will be a lwIP TCP echo server heading and some network information.

9. Set the computer's network setting to work with the Anvyl:
    a. Navigate start -> control panel -> network and sharing center -> change adapter settings (left side).
    b. Right click wired network connection (Local Area Connection) , click properties.
    c. In window, select Internet Protocol Version 4 (TCP/IPv4) then click the properties button.
    d. Click the radio button "use the follow IP address:"
    e. Settings:
        i. IP: 192.168.1.33
        ii. Subnet mask: 255.255.255.0
        iii. Gateway: 192.168.1.1
    f. Click the radio button "use the following DNS server addresses:"
    g. Setting:
        i. Preferred DNS server: 192.168.1.1

10. Ping to check that the IP address is correct
    a. Ping the Anvyl from windows cmd.exe
        i. "ping 192.168.1.10"

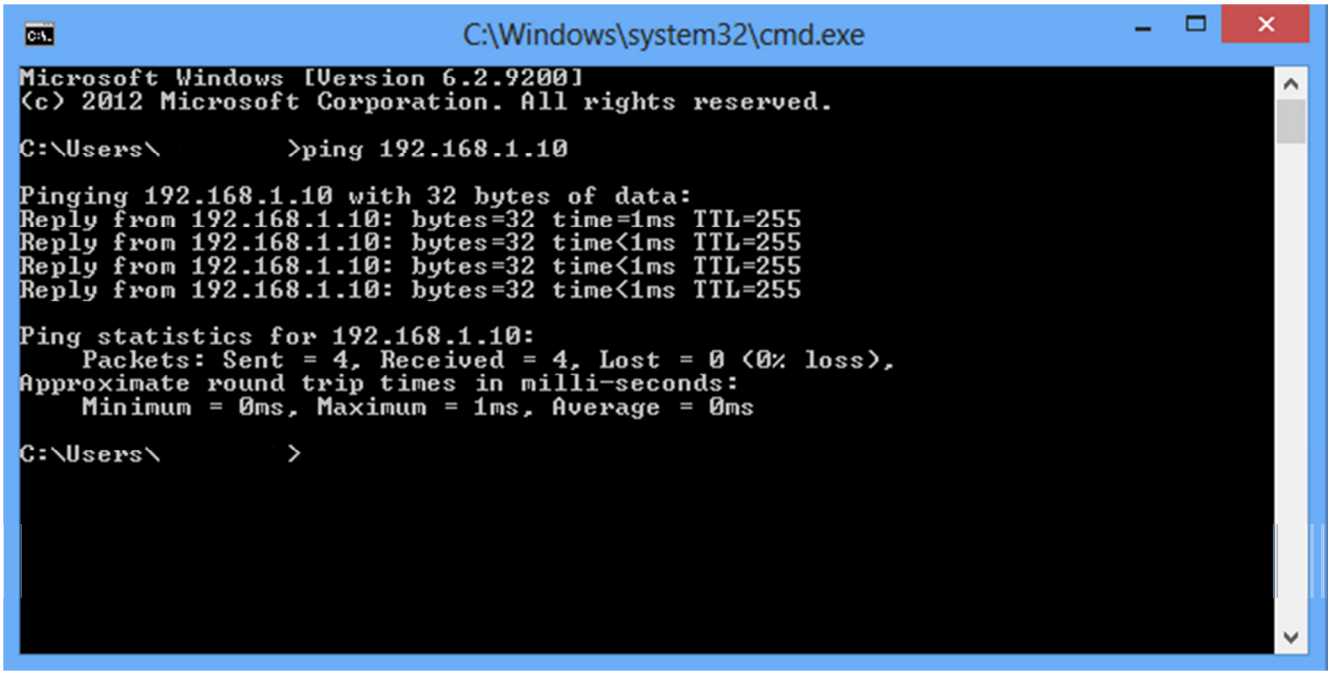

Fig. 10. *Ping the server.*

11. Through a telnet client, connect to the echo server
    a. Host: 192.168.1.10
    b. Port: 7

Now anything that is typed in the telnet terminal will be repeated. The example window shows the results of typing "This is a test."

Fig. 11. *Echo Server "This is a test."*

Chapter 11: LWIP Demo

This is an EDK project based on MicroBlaze. It involves the axi_ethernetlite, mii_to_rmii, AXI_INTC and AXI_TIMER pcores from Xilinx. The demonstration utilizes the echo server again, but also includes an ftp server and http server.

Additional Hardware Required:
- Ethernet cable (with RJ 45 connector)

Software Platform:
- Xilinx EDK 13.4
- Telnet client

Supplied Files:
- Programming bit file
- ISE EDK files
- Documents about the project

Instructions:
1. Plug an Ethernet cable from the computer to the Ethernet port on the Anvyl (J17)
2. Setup and program the board as described in the "Setting up and programming the Anvyl" section
3. Open a hyper terminal and select the corresponding COM port.
    a. Put the baud rate: 115200
    b. parity: none
    c. data bit: 8
    d. flow control: none
    e. stop: 1 bit
4. Navigate to and run XMD as administrator. It is located at C:/Xilinx/14.4/ISE_DS/EDK/bin/nt/xmd.exe

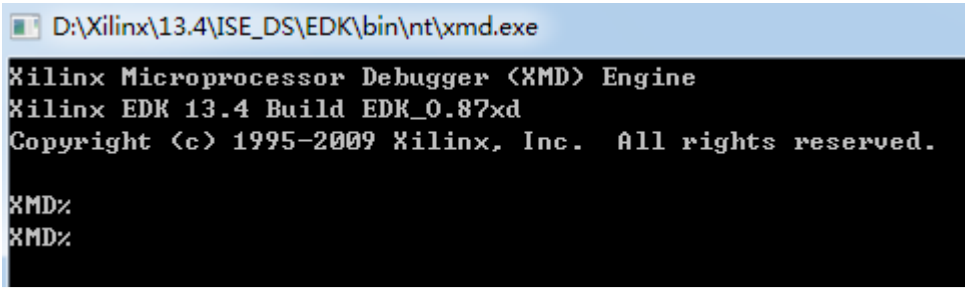

Fig. 12. x*md.exe.*

5. Connect to the MicroBlaze through JTAG
    a. "connect mb mdm"

```
XMD%
XMD% connect mb mdm

JTAG chain configuration
--------------------------------------------------
Device   ID Code         IR Length    Part Name
 1       44008093           6         XC6SLX45

MicroBlaze Processor Configuration :
-------------------------------------
Version.............................8.20.b
Optimization........................Performance
Interconnect........................PLB_v46
MMU Type............................No_MMU
No of PC Breakpoints................1
No of Read Addr/Data Watchpoints...0
No of Write Addr/Data Watchpoints..0
Instruction Cache Support..........off
Data Cache Support..................off
Exceptions  Support.................off
FPU  Support........................off
Hard Divider Support................off
Hard Multiplier Support............on - (Mul32)
Barrel Shifter Support..............on
MSR clr/set Instruction Support....on
Compare Instruction Support........on
Data Cache Write-back Support......off
Fault Tolerance Support............off
Stack Protection Support...........off

Connected to "mb" target. id = 0
Starting GDB server for "mb" target (id = 0) at TCP port no 1234
XMD%
```

Fig. 13. *Connect to MicroBlaze.*

6. Navigate to where the demo folder was placed
    a. Example for folder on desktop: “cd C:/Users/jsmith/Desktop/”Anvyl_Demos”/11.Anvyl_Ethernet_Demo/bitfile”

```
Connected to "mb" target. id = 0
Starting GDB server for "mb" target (id = 0) at TCP port no 1234
XMD% cd D:/hc_work/Anvyl/Anvyl_CD/02.Demos/11.Anvyl_LWIP_Demo/bitfile
XMD% ls
download.bit  image.mfs  raw_app.elf
```

Fig. 14. *Change the directory.*

7. Download the image file to a specific location in memory
    a. “dow –data image.mfs 0x88500000”

```
XMD% dow -data image.mfs 0x88500000
Downloading Data File -- image.mfs at 0x88500000
Progress ..................................................................
.....................................Done
XMD%
```

Fig. 15. *Download the image.mfs file to the Anvyl.*

8. Download the raw_app.elf file to the Anvyl
    a. “dow raw_app.elf”

```
XMD% dow raw_app.elf
Downloading Program -- raw_app.elf
        section, .vectors.reset: 0x00000000-0x00000007
        section, .vectors.sw_exception: 0x00000008-0x0000000f
        section, .vectors.interrupt: 0x00000010-0x00000017
        section, .vectors.hw_exception: 0x00000020-0x00000027
        section, .text: 0x88000000-0x880221cb
        section, .init: 0x880221cc-0x8802220b
        section, .fini: 0x8802220c-0x8802222b
        section, .ctors: 0x8802222c-0x88022233
        section, .dtors: 0x88022234-0x8802223b
        section, .rodata: 0x8802223c-0x88023f56
        section, .sdata2: 0x88023f57-0x88023f57
        section, .data: 0x88023f58-0x8802454b
        section, .eh_frame: 0x8802454c-0x8802454f
        section, .jcr: 0x88024550-0x88024553
        section, .bss: 0x88024558-0x880bfdf7
        section, .heap: 0x880bfdf8-0x881bfdf7
        section, .stack: 0x881bfdf8-0x882bfdf7
Setting PC with Program Start Address 0x00000000
System Reset .... DONE

XMD%
```

Fig. 16. *Downloading raw_app.elf.*

9. Run LWIP echo
    a. “run”

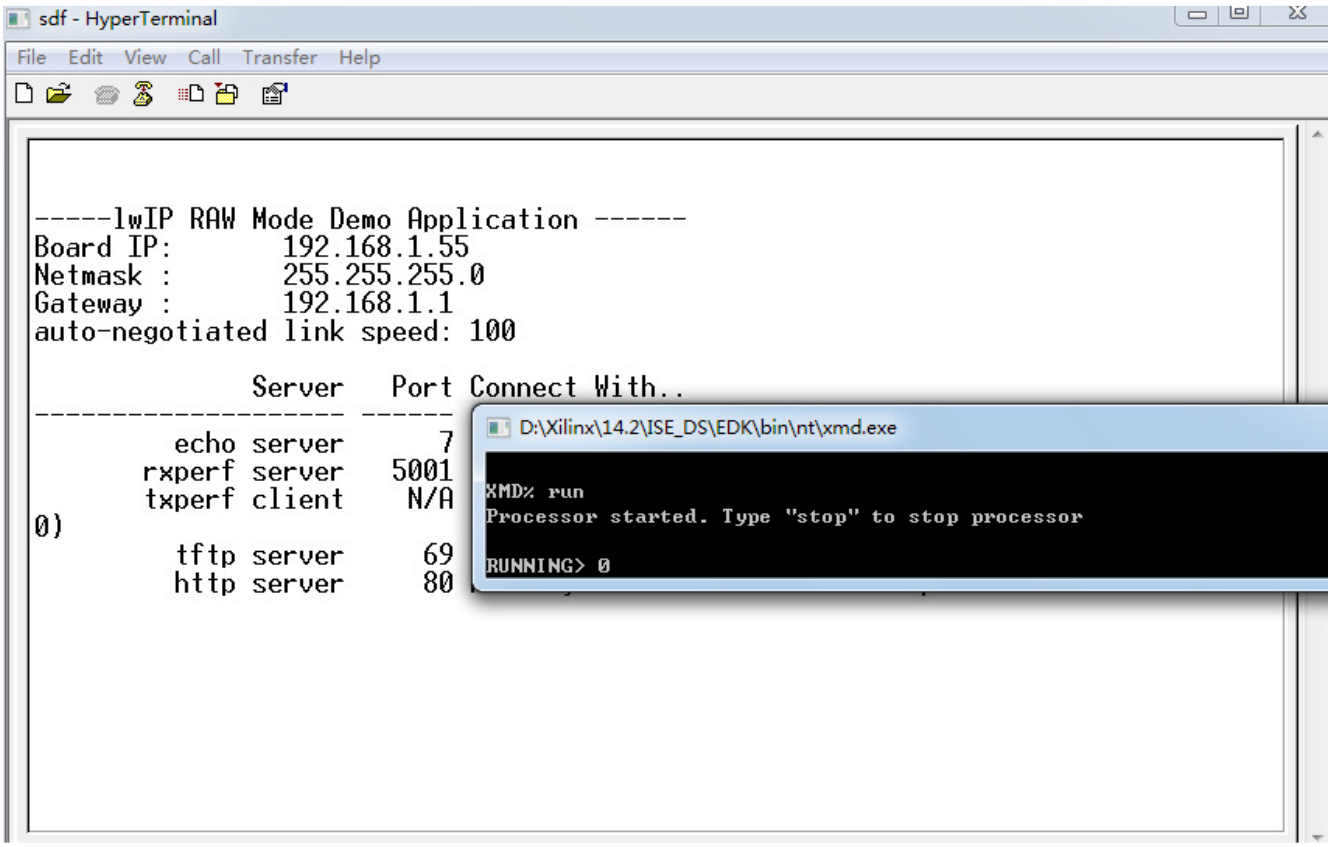

Fig. 17. *Run LWIP echo and Hyper Terminal.*

The LWIP echo server has been successfully run on the Anvyl. In the hyper terminal, there will be a lwIP TCP echo server heading and some network information.

10. Set the computer's network setting to work with the Anvyl:
    a. Navigate to: start -> control panel -> network and sharing center -> change adapter settings (left pane of the window).
    b. Right click wired network connection (Local Area Connection) and select properties.
    c. Select "Internet Protocol Version 4 (TCP/IPv4)" then click the properties button.
    d. Click the radio button "use the follow IP address:"
    e. Settings:
        i. IP: 192.168.1.33
        ii. Subnet mask: 255.255.255.0
        iii. Gateway: 192.168.1.1
    f. Click the radio button "use the following DNS server addresses:"
    g. Setting:
        i. Preferred DNS server: 192.168.1.1

11. Ping to check that the IP address is correct In windows command prompt
    a. Ping the Anvyl from windows cmd.exe
        i. "ping 192.168.1.55"

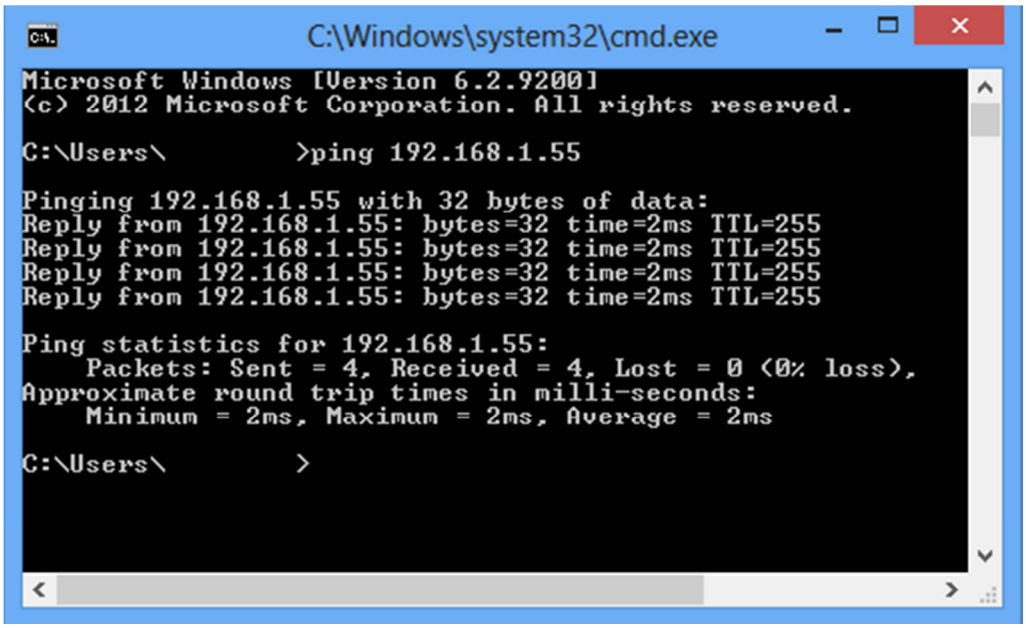

Fig. 18. *Ping the server at 192.168.1.55.*

12. Through a telnet client, connect to the echo server
    a. Host: 192.168.1.55
    b. Port: 7

Now anything that is typed in the telnet terminal will be repeated. The example window shows the results of typing “This is a test.”

Fig. 19. *Echo Server “This is a test.”*

13. Copy and paste this address into the address bar http://192.168.1.55 of a web browser.

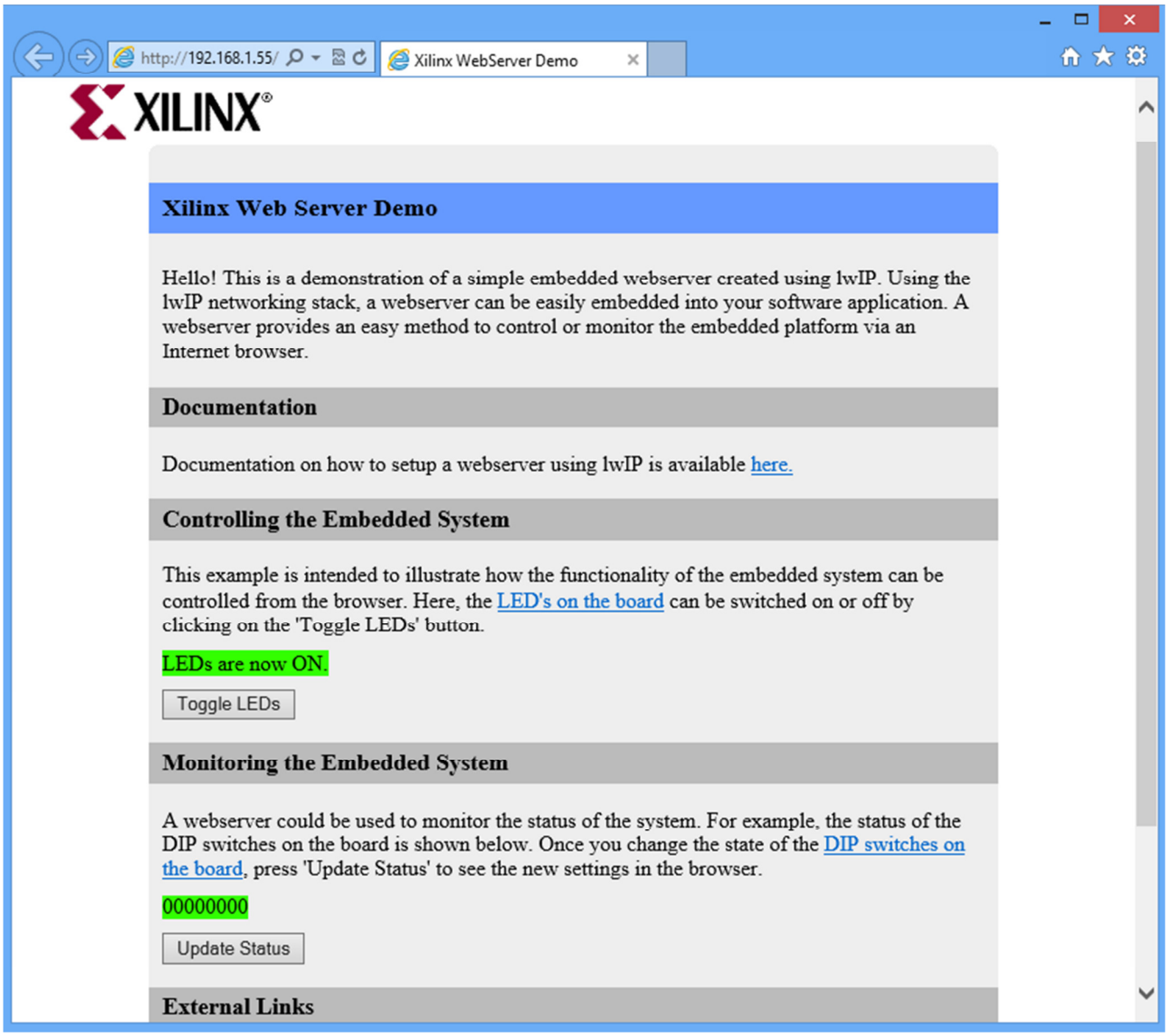

Fig. 20. *Anvyl Webserver.*

The Anvyl is hosting a webserver and from the http interface the user can toggle the LEDs and monitor the state of the user switches (SW0-7). Also, on this page, there are links to the Xilinx webpage.

Chapter 12: System Demo

The system demonstration brings together multiple aspects of the Anvyl board and demonstrates them at the same time. It shows capability of the TFT touchscreen, the seven segment display, the keypad, HDMI output, VGA output, onboard switches and LEDs.

Additional Hardware Required:

- VGA cable
- HDMI cable or HDMI to DVI cable
- HDMI/DVI and VGA capable monitor

Software Platforms:

- Xilinx EDK 13.4
- Hyper terminal client

Supplied Files:

- Programming bit file
- EDK project files

Instructions:

1. Open a hyper terminal
    b. settings:
        - Baud rate: 115200
        - Data bit: 8 bit
        - Parity: none
        - Stop bit: 1 bit

2. Setup and program the board as described in the “Setting up and programming the Anvyl” section

When the Anvyl has been programmed successfully, there will be “Welcome to Anvyl.” in the hyper terminal window. The OLED will switch through three different pictures displaying text or pictures. The VGA(640 x 480 @60Hz) and HDMI(1280 x 720 @60Hz) outputs are a vertical red and green pattern with a moving Digilent logo. The TFT touch screen will react to being touched and switch 8 (SW8) will control the backlight. When pressure is applied to the touch screen, LEDs 9-14 (LD9-LD14) will light up. Switches 0-7 (SW0-7) toggles LEDs 0-7(LD0-7). Pressing buttons on the keypad will change how the seven segment display displays characters.

Chapter 13: PmodAD1 Demo

The PmodAD1 is an analog to digital converter with a sampling rate of one million samples per second.

Additional Hardware Required:
- PmodAD1
- Signal generator

Software Platforms:
- Xilinx ISE 13.4

Supplied Files:
- Programming bit file
- ISE project files
- Documents for PmodAD1

Instructions:
1. Connect the PmodAD1 to the lower row of the JC Pmod header on the Anvyl
2. Connect the signal generator to PmodAD1
    a. Signal to PmodAD1 J2 position 1
    b. Ground to PmodAD1 J2 position 5
3. Setup and program the board as described in the "Setting up and programming the Anvyl" section
4. Start the signal generator with a signal between 0-3.3V
5. Push button 0 (BTN0) to read from the signal generator

The 8 user LEDs will illuminate to indicate that PmodAD1 is working. LED 14 (LD14) will illuminate when data collection is done.
Note: When users push button 0 (BTN0), LED 14 (LD14) will turn off

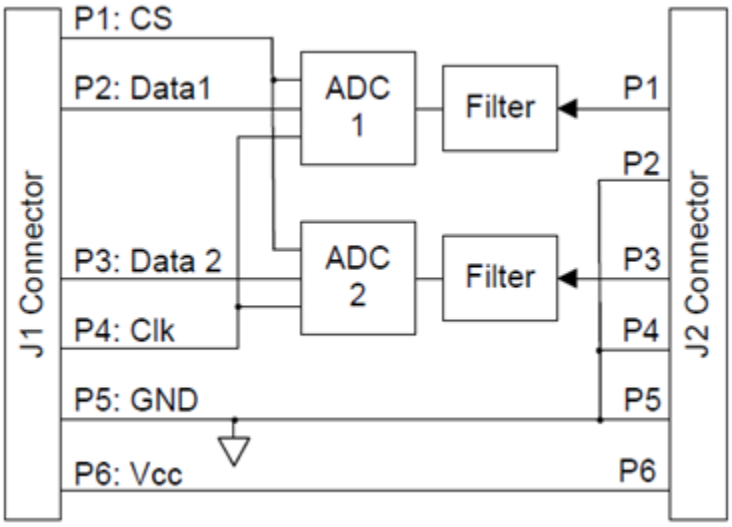

Fig. 21. AD1 Circuit Diagram.

Chapter 14: PmodDA2 Demo

The PmodDA2 produces an analog voltage from 0-3.3V from a digital signal along two different channels.

Additional Hardware Required:
- PmodAD2
- Oscilloscope

Software Platforms:
- Xilinx ISE 13.4

Supplied Files:
- Programming bit file
- ISE project files
- Documents about PmodDA2

Instructions:
1. Connect the PmodDA2 to lower row of Pmod header JE on the Anvyl
2. Connect the oscilloscope to PmodDA2
    a. Oscilloscope signal to jumper 2 position 1
    a. Oscilloscope ground to jumper 2 position 5
6. Setup and program the board as described in the "Setting up and programming the Anvyl" section

The switches 0-7 (SW0-7) change the waveform reading on the oscilloscope. Button 0 (BTN0) updates the value set by the switches to the PmodDA2.

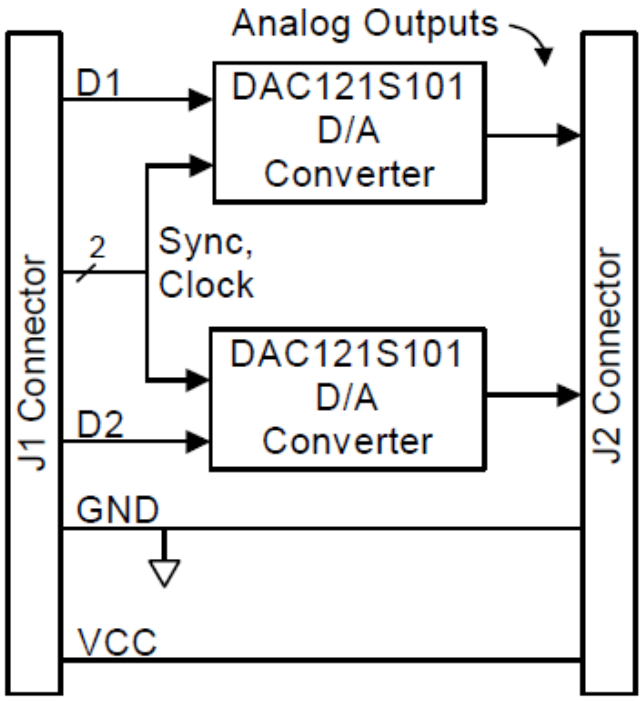

Fig. 22. *PmodDA2 schematic.*

Chapter 15: PmodHB3 Demo

The PmodHB3 is an ideal solution for projects that need a logic signal to drive a DC motor.

Additional Hardware Required:
- PmodHB3
- Motor or other load

Software Platform:
- Xilinx ISE 13.4

Supplied Files:
- Programming bit file
- ISE project files
- Documents about PmodHB3

Instructions:
1. Connect the PmodHB3 to the lower row of the JG Pmod header
2. Connect the motor Vdd and ground to M+ and M- of the PmodHB3 respectively
3. Connect a power supply suitable for the selected motor to Vdd and GND of the Pmod
4. Setup and program the board as described in the "Setting up and programming the Anvyl" section

The motor can now be controlled using the switches. Switches 0-6 (SW0-6) control the pulse width signal for the motor. Switch 7 (SW7) changes the direction of the motor. Button 3(BTN3) can be used as a reset.

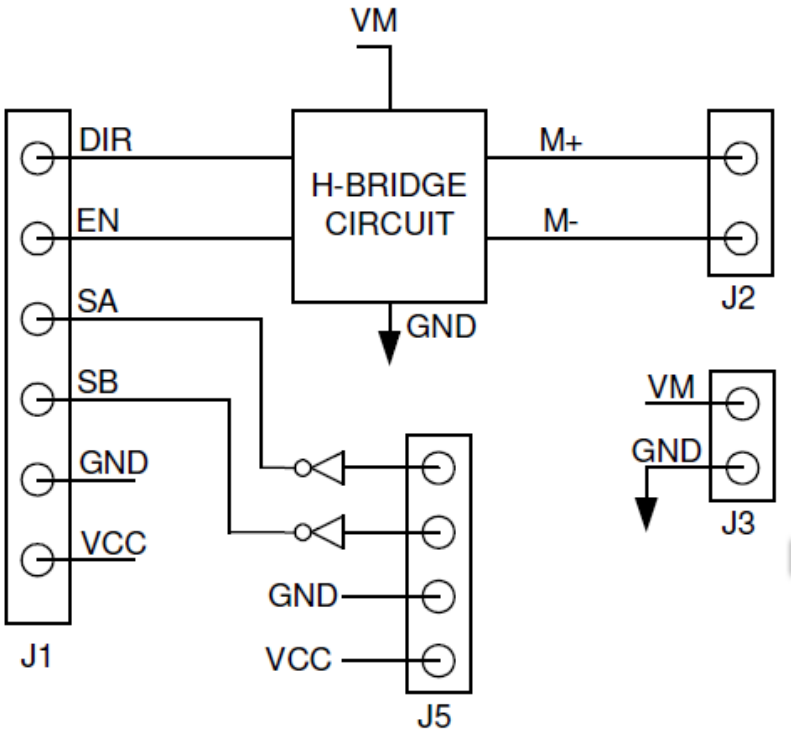

Fig. 23. *PmodHB3 Schematic*.

Chapter 16: PmodOD1 Demo

The PmodOD1 is an open drain module board and can drive high current devices using an on board power FET.

Additional Hardware Needed:
- PmodOD1
- DC motor or other load

Software Platform:
- Xilinx ISE 13.4

Supplied Files:
- Programming bit file
- ISE project files
- Doc about PmodOD1

Instructions:
1. Connect the PmodOD1 to lower row of the JA Pmod header
5. Connect the motor to VL (+) and any OD (OD1-4) (-)
6. Setup and program the board as described in the “Setting up and programming the Anvyl” section.
2. The PmodOD1 is controlled with switches(SW0-3)
    a. SW0 turns on OD1 port
    b. SW1 turns on OD2 port
    c. SW2 turns on OD3 port
    d. SW4 turns on OD4 port

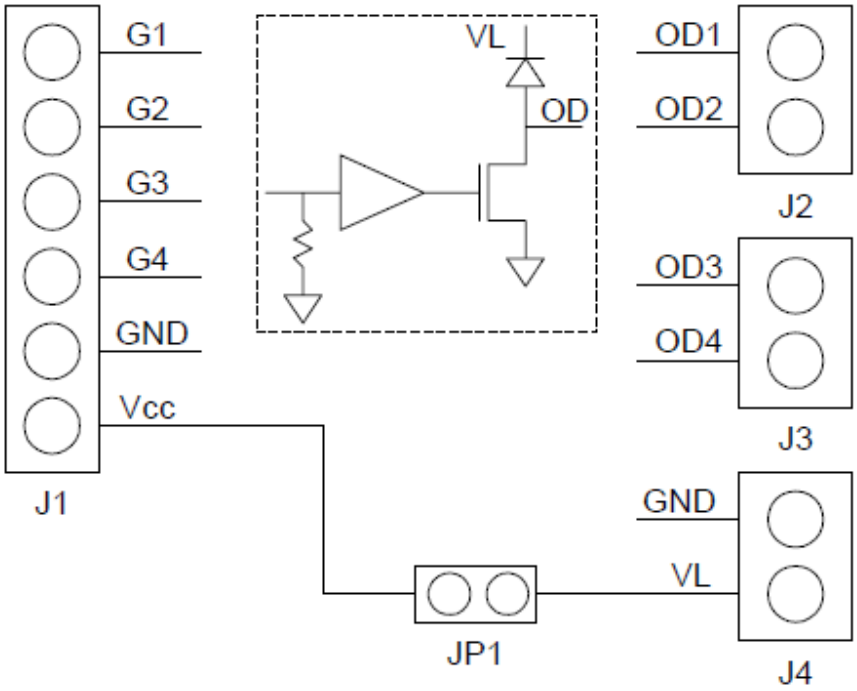

Fig. 24. *OD1Pmod Schematic.*

Chapter 17: USB-HID Keyboard Demo

This demo connects a USB keyboard with the Anvyl and prints corresponding key presses to a hyper terminal connection.

Additional Hardware Required:
- USB Keyboard

Software Platform:
- Xilinx EDK 13.4

Supplied files:
- Programming bit file
- ISE EDK files

Instructions:
1. Connect the USB Keyboard to J14
2. Open a hyper terminal
    a. settings:
        - Baud rate: 115200
        - Data bit: 8 bit
        - Parity: none
        - Stop bit: 1 bit
3. Setup and program the board as described in the “Setting up and programming the Anvyl” section.

When any button is pressed on the keyboard, the Hyper Terminal will show “Data received from PS2_1 Keyboard=(corresponding keyboard code)”. During typing, LED 16 (LD16) will be showing data transfer.

Chapter 18: Digital Audio Demo

This demo shows how the board can generate audio through the headphone or line out ports on the Anvyl.

Additional Hardware Required:
- Speaker

Software Platform:
- Xilinx EDK 13.4

Supplied files:
- Programming bit file
- ISE EDK files
- SDK code contains CODEC configuration
- Documentation on the codec chip

Instructions:
1. Connect the speaker to “LINE OUT” port (J7) or to “HEADPHONE” port (J6)
2. Move all user switches (SW0-7) to the down or low position on the board.
3. Setup and program the board as described in the “Setting up and programming the Anvyl” section. Ignore the switch configuration instructions.

Once programmed, the board will play sound through the “LINE OUT” port or the “HEADPHONE” port when buttons 0-2 (BT0-2) are pressed.