

Overview

This document describes the AD1 VHDL reference component used to interface a Digilent PmodAD1 with a Digilent FPGA development board. The core issue is correctly timing the synchronization of data communications between the development board and the PmodAD1.

The component inputs a digital signal serially from the PmodAD1 and outputs the data to any external VHDL component. It also supplies the appropriate timing sequence to clock the PmodAD1 board.

Communications timing is developed and a finite state machine is designed to model the component.

Features include:

- Using the PmodAD1 board to take in a 16-bit vector serially using the correct timing sequence.
- Outputting a 12-bit vector with the converted digital value.

Functional Description

Component Architecture

The VHDL component is an entity named AD1RefComp which has five inputs and five outputs. The input ports are a 50MHz clock and an asynchronous reset button along with the data from the ADCS7476 that is serially shifted in on each clock cycle (SDATA1 and SDATA2). The outputs are the SCLK signal which clocks the PmodAD1 board at 12.5MHz and a chip select signal (nCS) that enables the ADCS7476 chips on the PmodAD1 board as well as two 12-bit output vectors labeled DATA1 and DATA2, coming from the ADCS7476 chips. The START input signal is used to tell the component when to start a conversion. After a conversion is done the component activates the DONE output signal. A block diagram of the component is shown in Figure 1.

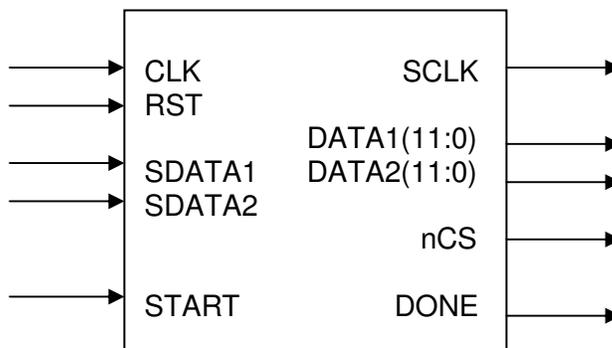


Figure 1 PmodAD1 Reference Component

Timing

Figure 1 of the ADCS7476 Data Sheet (<http://www.national.com/ds/DC/ADCS7476.pdf>) was used to determine the timing sequence needed to generate 16 bits of data using the two ADCS7476 chips inside the PmodAD1 board. The signal nCS must be at a low or zero state while the data is generated on the falling edge of the clock signal. Immediately following the transfer of data, the signal nCS must be driven high to signal when a new set of data can be generated.

State Machine

The logic that created the timing sequence to take in the data inputs SDATA1 and SDATA2 serially and latch in the 16-bit vector as well as clock the nCS and SCLK outputs, was designed by creating a finite state machine. The finite state machine created is shown in Figure 2.

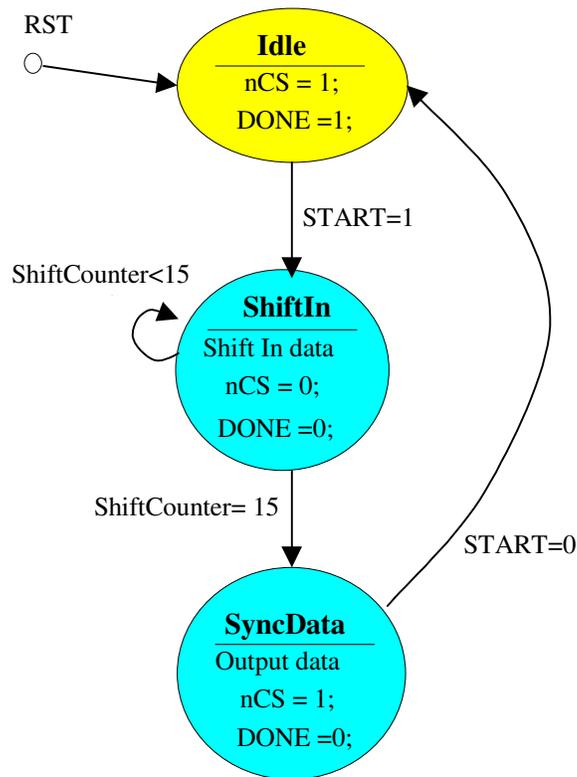


Figure 2 FSM of PmodAD1 Reference Component

There are three states labeled “Idle”, “ShiftIn”, and “SyncData” respectively. During the Idle state, the DONE output signal needs to be high in order to allow a conversion. When the START signal is going high, the state machine goes on to ShiftIn state. In this state the DONE signal goes low, and the data from the PmodAD1 board is serially shifted in from MSB to LSB for 16 clock cycles to ensure that all the 16 bits of data have been received from each chip. After shifting is done, the state machine goes in the SyncData state. In this state the data received from the PmodAD1 is placed on the 12-bit output ports DATA1 and DATA 2 . If the START input signal is low, the machine goes back to the Idle state, ready to accept another conversion.

No matter what the current state is, the RST input signal resets the state machine and puts it in the Idle state.